Digital Electronics

Answer Sheet 8

1. Normally, efficient implementations use fewer gates and/or devices and are therefore cheaper. Chip count can also be a factor with efficiency falling for increasing numbers of chips.

2. $\overline{A}BCD + A\overline{B}\overline{C}D + ABCD + \overline{A}B\overline{C}D + \overline{A}\overline{B}\overline{C}\overline{D} + \overline{A}\overline{B}CD + A\overline{B}CD$

A	B	C	D	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

	Col 0 Cells 0-7	Col 1 Cells 8-15	Col 2 Cells 16-23	Col 3 Cells 24-31	Col 4 Cells 32-39	Col 5 Cells 40-47	Col 6 Cells 48-55	Col 7 Cells 56-63
Row 0	0	0	X	X	X	X	X	X
Row 1	1	1	X	X	X	X	X	X
Row 2	0	0	X	X	X	X	X	X
Row 3	1	1	X	X	X	X	X	X
Row 4	0	0	X	X	X	X	X	X
Row 5	1	0	X	X	X	X	X	X
Row 6	0	0	X	X	X	X	X	X
Row 7	1	1	X	X	X	X	X	X

Notes:

- In general, a large number of product terms can be implemented more efficiently in ROM.
- For implementation in gates, the above function can be minimised to improve the efficiency of the implementation
- The use of a 1 x 64-bit ROM is wasteful of 75% of the storage but, depending on the application constraints, the ROM implementation may still be preferred; for example, if it is necessary to frequently change the logic, this can most easily be done by reprogramming an EPROM.