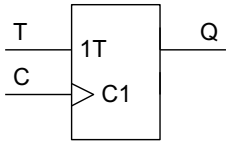
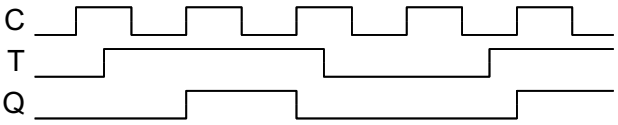
E2.1 – Digital Electronics II

Problem Sheet 4 –Timing Constraints

(Question ratings: A=Easy, …, E=Hard. All students should do questions rated A, B or C as a minimum)

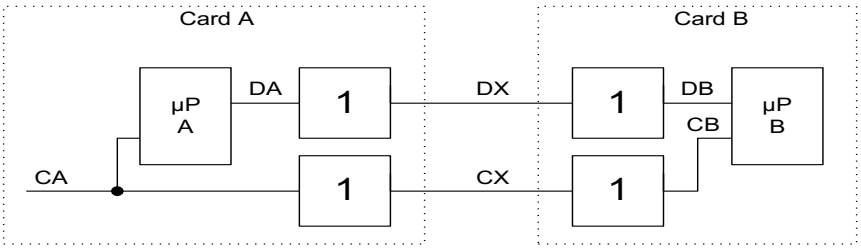
1B. A toggle flipflop (T-flipflop) changes state whenever its T input is high on the CLOCK ↑ edge as shown in the timing diagram.



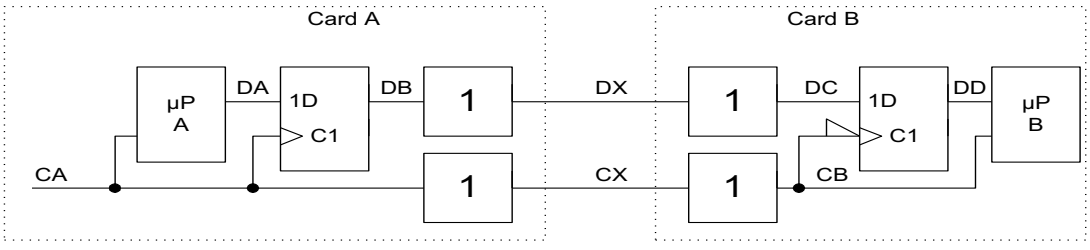


Show how a T-flipflop can be made by combining an XOR gate with a D-flipflop.

2C. A multi-processor system contains two microprocessors which are mounted on separate printed circuit cards. The clock and data signals pass through a line driver when they leave one card and a line receiver when they pass onto the next. The combined delay of the driver+receiver may vary between 13 ns and 22 ns. New data values appear at DA on the falling edge of CA with a propagation delay of 5 to 50 ns. Data is clocked into µP B on the rising edge of CB with a setup time of 12 ns and a hold time of 27 ns. If the clock, CA, is a symmetrical squarewave, calculate its maximum frequency.



3C. We can speed up the circuit from the previous question by using high-speed flipflops with shorter propagation delays and setup times. The flipflops in the revised circuit have setup and hold times of 5 ns and 3 ns and propagation delays in the range 2 to 10 ns. Note that the second flipflop has an inverted clock. Calculate the new maximum clock frequency by considering its minimum period for each of µPA→flipflop, flipflop→flipflop and flipflop→µPB.



4C. By considering the Hold requirements, explain why the circuit in question 3 would not work if the two flipflops were interchanged.

5D. If we add a third flipflop, we can improve the speed further. Calculate the maximum clock frequency for the following circuit and explain in words how it has achieved the performance increase when compared with the original circuit of question 2.