§10 - MEMORY INTERFACING

10.1 Introduction

Figure 8.1 shows a summary of the main characteristics of different types of memories. These are:

- ? SDRAM - Synchronous Dynamic RAM
- ? DRAM - Dynamic RAM
- ? SRAM - Static RAM
- ? EEPROM/Flash RAM - Electrically eraseable PROM/ Flash RAM

In this part of the course, we will examine briefly the internal organisation of memory devices, interfacing to static RAM, dynamic RAM etc., how to read timing diagrams, the many different modes of dynamic RAM (and why they are useful), and interfacing memory to microprocessors.

characteristic	SDRAM	DRAM	SRAM	Flash RAM
Trans per cell	1.5	1.5	4-6	1
Relative size	1.5	1.5	4-6	1-1.5
Density	256M	64M	16M	64M
Overhead	Refresh	refresh	none	Block erase
Volatile	yes	yes	yes	no
Data retention	64ms	64ms	?	10 yrs
In-system alterable	yes	yes	yes	yes
no of reprogram	?	?	?	>100,000
Typical write speed	7 – 35 ns	30-90ns	7 – 10 ns	6s (32KW)
Typical read time (ns)	7 – 35 ns	30-90ns	7 – 10 ns	80 – 110 ns

Figure 10.1 Characteristics of memory types

10.2 **Static RAM**

The basic per-bit static RAM cells (CMOS) is shown in figure 10.2. It consists of 6 transistors connected as cross-coupled inverters (forming a bistable circuit). The ***word line*** is active when the cell is accessed. The cell drives a complimentary pair of ***bit lines***. The advantages of using two bit lines are to reduce noise (any common-mode noise are rejected) and to make the write operation easier.

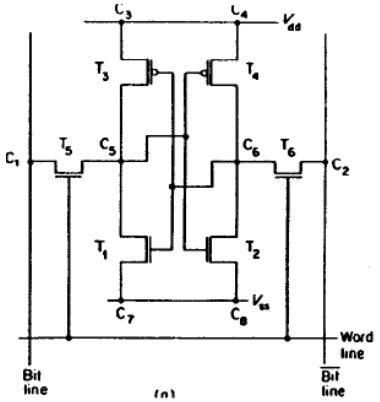


Figure 10.2 A CMOS static RAM cell

Memory cells in all devices are arranged as square array to save space and to minimize the address decoding circuits. The internal organisation of a 4K static RAM device is shown in figure 10.3.

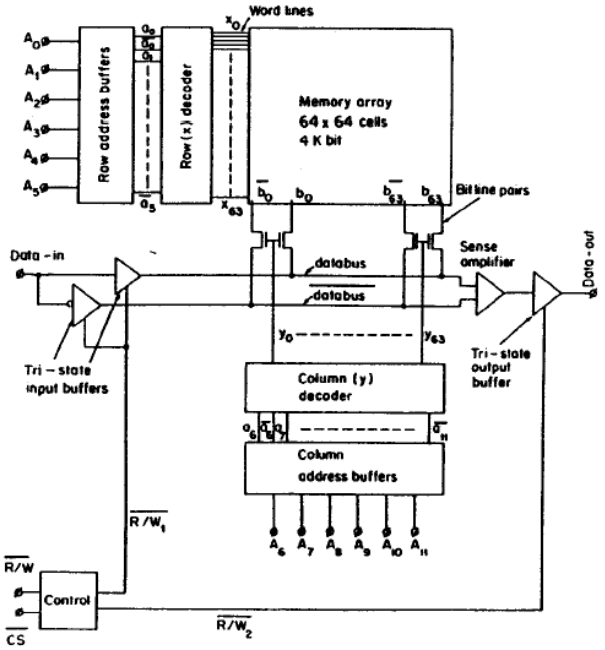


Figure 10.3 Block Diagram of a 4k static RAM

10.2.1 Static Memory Signals

In order to design with static RAM devices, you must be able to interpret the timing diagram for read and write cycles which are specified on data sheets. In a memory system, there will be signals flowing bewteen the processor and the memory devices. The signals from the processor to the memory are:

* *addresses* - indicating the memory locations selected.
* *write enable* - chooses bewteen read or write mode, also forces the write operation.
* *chip select(s)* - select one of many possible memory chips in a system. This signal is usually supplied by the address decoder circuit. If chip select is OFF the memory is deselected.
* *output enable* - used to control the output buffer.
* *data input* - data to be written to memory.

In contrast, the only data from memory to the processor is the output data. For memory devices with wide datapath (e.g. byte-wide memory), input and output data signals are usually common. Figure 10.4 shows the block diagram of Motorola's 64Kx1 static RAM chip:-

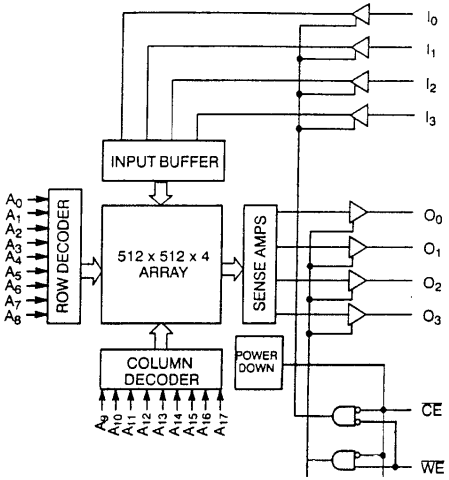


Figure 10.4 Cypress 256K x 4 Fast Static RAM

10.2.2 Static Memory Timing Diagrams

Timing diagrams specify the minimum required and maximum expected timing for a system to function properly. Two sets of timing symbols are shown in figure 10.5 & 10.8. The first is the JEDEC standard symbols which is more meaningful. The second is older but is still commonly used.

A timing diagram for a basic read cycle during which the processor reads out information stored in a static RAM is shown in figure 8.4. The read cycle operation consists of:

1. System selects the RAM by turning the chip enable on (E low)
2. System sets the correct addresses (A set)
3. System turns the output enable on (G low)
4. System must make sure that the time that old data from ohter sources on the data bus must disappear within the minimum of t_{GLQX} or t_{ELQX}.
5. System must wait a minimum time of t_{AA}, t_{AC}, or t_{OE} in order to be sure that correct data is read.

READ CYCLE

Parameter	Symbol		Min	Max	Min	Max	Min	Max	Unit
	Standard	Alternate							
Read Cycle Time	t_{AVAV}	t_{RC}	25	–	30	–	35	–	ns
Address Access Time	t_{AVQV}	t_{AA}	–	25	–	30	–	35	ns
Chip Enable Access Time	t_{ELQV}	t_{ACS}	–	25	–	30	–	35	ns
Output Enable Access Time	t_{GLQV}	t_{OE}	–	12	–	15	–	15	ns
Output Hold from Address Change	t_{AXQX}	t_{OH}	5	–	5	–	5	–	ns
Chip Enable Low to Output Active	t_{ELQX}	t_{LZ}	5	–	7	–	10	–	ns
Chip Enable High to Output High-Z	t_{EHQZ}	t_{HZ}	0	10	0	12	0	15	ns
Output Enable Low to Output Active	t_{GLQX}	t_{LZ}	5	–	5	–	10	–	ns
Output Enable High to Output High Z	t_{GHQZ}	t_{HZ}	0	10	0	12	0	15	ns

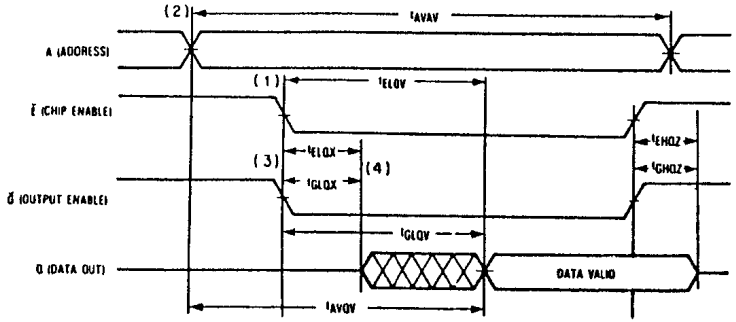


Figure 10.5 Typical Read cycle timing diagram for static RAM

A simple write cycle consists of:

1. System sets correct addresses (A set)
2. System selects the RAM by turning the chip enable on (E low)
3. System waits a minimum required amount of time after changing addresses for RAM to perform internal 'set up' of addresses t_{AVWL} , then turns the write enable on (W low)
4. System waits for a minimum of t_{WLQZ} after the write enable signal to make sure that the RAM output driver is disabled.
5. System output new data on bus for at least t_{DVWH} before write enable is take high
6. The write enable pulse width must be a minimum of t_{WLWH} to ensure correct writing to RAM.

Figure 10.6 shows a typical timing diagram for a write cycle.

WRITE CYCLE

Parameter	Symbol		Min	Max	Min	Max	Min	Max	Unit
	Standard	Alternate							
Write Cycle Time	t_{AVAV}	t_{WC}	25	—	30	—	35	—	ns
Address Setup Time	t_{AVWL}	t_{AS}	0	—	0	—	0	—	ns
Address Valid to End of Write	t_{AVWH}	t_{AW}	20	—	25	—	30	—	ns
Write Pulse Width	t_{WLWH}	t_{WP}	20	—	25	—	30	—	ns
Data Valid to End of Write	t_{DVWH}	t_{DW}	10	—	12	—	15	—	ns
Data Hold Time	t_{WHDX}	t_{DH}	0	—	0	—	0	—	ns
Write Low to Output High-Z	t_{WLOZ}	t_{WZ}	0	10	0	12	0	15	ns
Write High to Output Active	t_{WHOX}	t_{OW}	5	—	8	—	10	—	ns
Write Recovery Time	t_{WHAX}	t_{WR}	0		0		0		ns

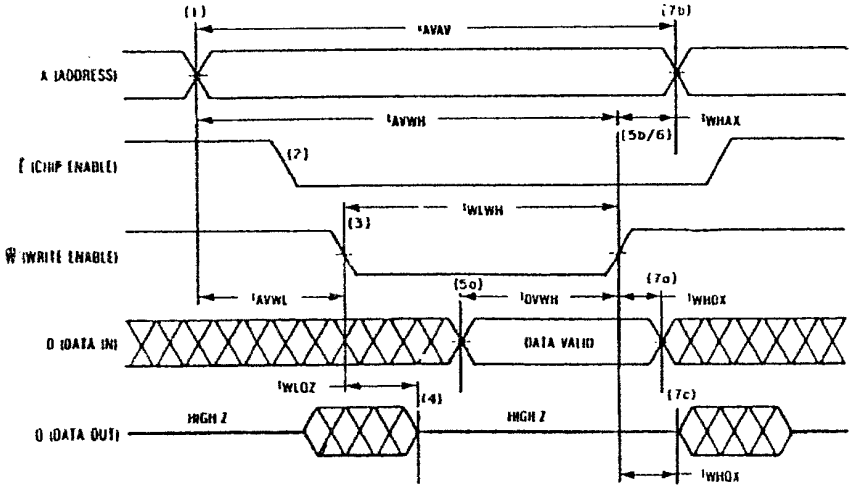


Figure 10.6 Typical Write Cycle Timing

10.2.3 Memory Organisation

Memory can be organised in various ways: bit-wide, nibble-wide, byte-wide, 16/18-bit or 32/36 bit wide. Figure 10.7 shows the selection table from the current Micron fast CMOS SRAM data book. To ensure that memory chips from different manufacturers are interchangeable, the Electronic Industry Association (EIA) publishes a JEDEC standard on pinout for different types of memories (SRAM, DRAM, SDRAM etc.).

Density	Memory Configuration	Part Number	Flow-Through[10]	Pipelined SCD[11]	Pipelined DCD[11]	Die Rev.	I/O Voltage	Package[12]	Pins
1Mb	64K x 18	MT58L64L18	F	P	D	None	3.3V	T	100
	32K x 32/36	MT58L32L32/36	F	P	D	None	3.3V	T	100
2Mb	128K x 18	MT58L128L18	F	P	D	None	3.3V	T or F	100
	128K x 18	MT58L128V18	F	P	D	None	2.5V	T or F	100
	64K x 32/36	MT58L64L32/36	F	P	D	None	3.3V	T or F	100
	64K x 32/36	MT58L64V32/36	F	P	D	None	2.5V	T or F	100
4Mb	256K x 18	MT58L256L18	F	P	D	1	3.3V	T or F	100/165
	256K x 18	MT58L256V18	F	P	D	1	2.5V	T or F	100/165
	128K x 32/36	MT58L128L32/36	F	P	D	1	3.3V	T or F	100/165
	128K x 32/36	MT58L128V32/36	F	P	D	1	2.5V	T or F	100/165
8Mb	512K x 18	MT58L512L18	F	P	D	None	3.3V	T, S, or F	100/165
	512K x 18	MT58L512V18	F	P	D	None	2.5V	T, S, or F	100/165
	256K x 32/36	MT58L256L32/36	F	P	D	None	3.3V	T, S, or F	100/165
	256K x 32/36	MT58L256V32/36	F	P	D	None	2.5V	T, S, or F	100/165
16Mb	1 Meg x 18	MT58L1MY18	F	P	D	None	3.3V/2.5V	T or F	100/165
	1 Meg x 18	MT58L1MV18	F	P	D	None	2.5V	T or F	100/165
	512K x 32/36	MT58L512Y32/36	F	P	D	None	3.3V/2.5V	T or F	100/165
	512K x 32/36	MT58L512V32/36	F	P	D	None	2.5V	T or F	100/165

Figure 10.7 Part Listing of Motorola current FAST SRAM selection table

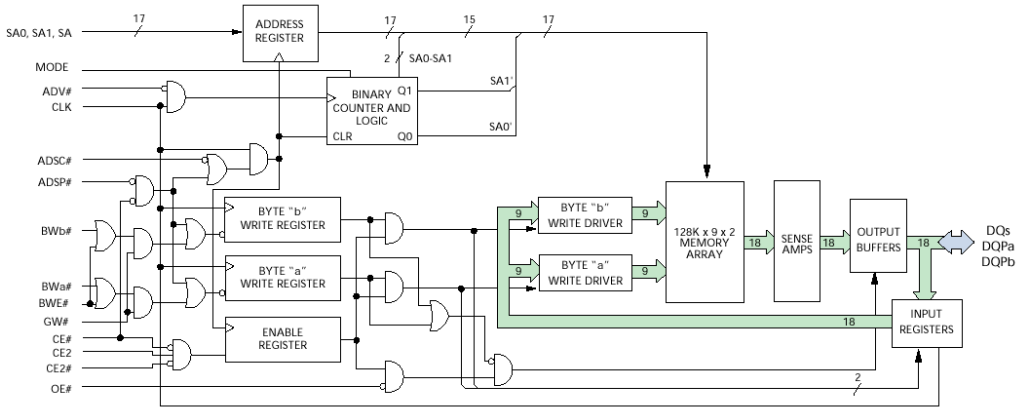


Figure 10.8 Block Diagram of MCM6264 8Kx8 memory

10.3 Design Example 1: Address Decoding

Consider the problem of implementing the following memory map for an 8-bit microprocessor based system (Figure 10.9).

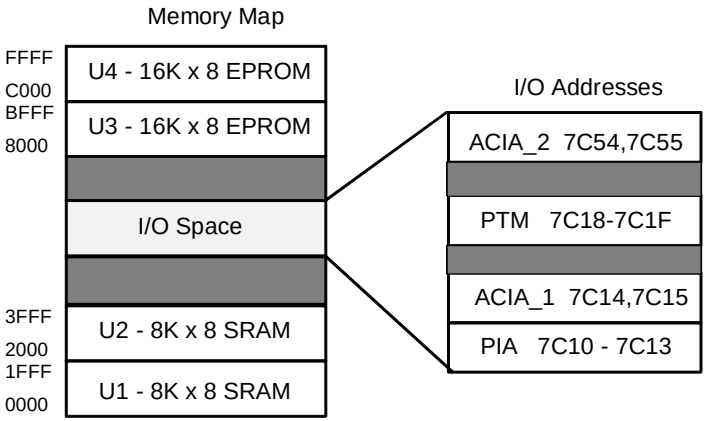


Figure 10.9 6Simple System Memory Map

A decoder circuit is needed to generate the necessary chip select signals to the memory devices and peripheral chips. For example, the chip select for U4 has to generate the signal: CS_U1 = / (/A15*/A14*/A13). (Note that all chip select signals are low active.) Since the peripheral circuits occupies small blocks of the memory space, decoding their select signals take more address lines. For the PIA, for example, we need to decode 14 of the 16 address lines. (Only A0 and A1 are don't cares.) To fully decode the addresses, the best option is to use a PLD. For example, the FPLA 82S103 has 16 inputs and 9 macrocells (i.e. 9 outputs). It could therefore decode any addresses needed. Alternatively, two level of decoding could be used as shown in figure 8.10. Here two EPLDs are used, the first decodes the upper address bits for the memory chips, and the second decodes the low address bits for the I/O map.

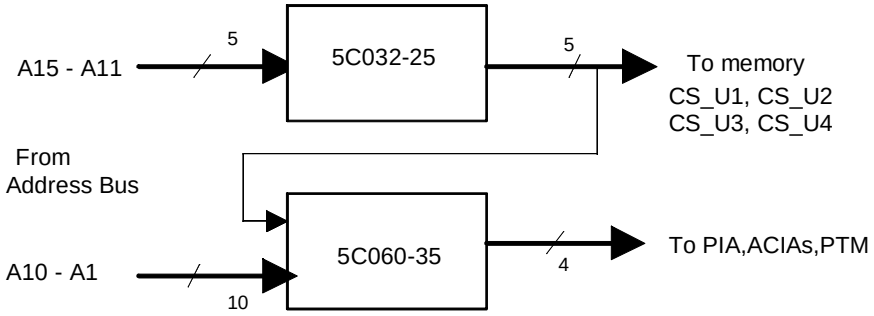


Figure 10.10 EPLD Decoders

The EPLD decoder could be made to work faster if we gate the outputs from the two EPLD using a NAND gate. (See figure 10.11).

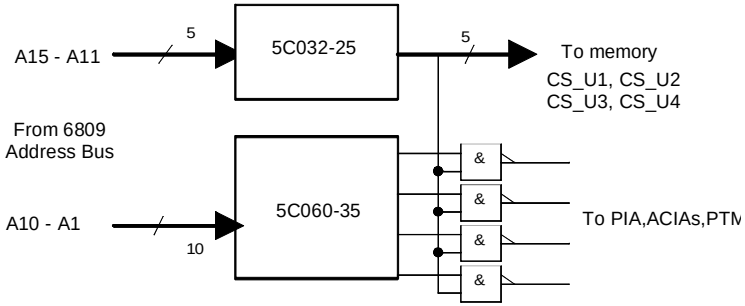


Figure 10.11 EPLD Decoders - With gating

10.5 Design Example 3: 68000 Memory Interfacing

Let us next consider memory interface for the 68000 processor. Figure 10.19 shows a (simple) memory interface circuit.

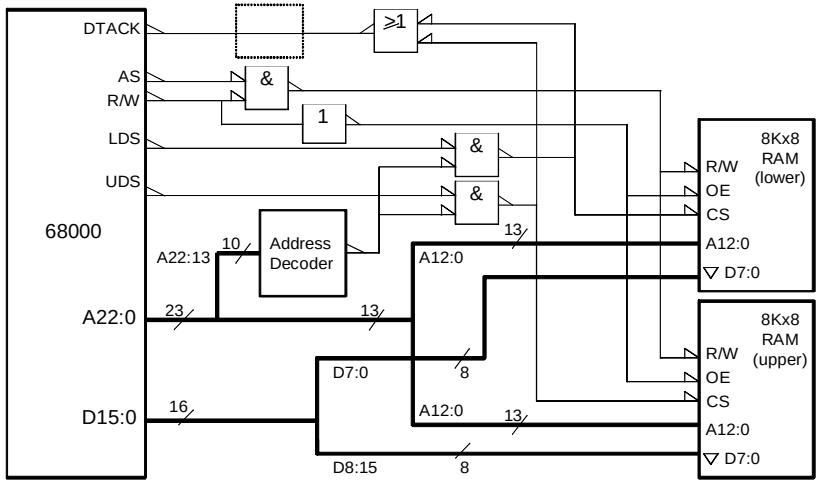


Figure 10.19 68000 Memory Interface Circuit

Note the following:

* 68000 has 23 bit address bus and 16-bit data bus.
* The address bus is supported by the Address Strobe (AS) signal which goes active after the address becomes valid.
* Byte addressing and word addressing are both supported. The Lower/Upper Data Strobe signals (LDS, UDS) are used to indicate which whether lower/upper bytes, or both, are transferred. The meaning of LDS and UDS signals are described by the following table:

UDS	LDS	Operation	D15:8	D7:0
Negated	Negated	No Op	*Invalid*	*Invalid*
Negated	Asserted	Write lower byte	*Invalid*	lower byte data
Asserted	Negated	Write upper byte	upper byte data	*Invalid*
Asserted	Asserted	Write word	upper byte data	lower byte data

* 68000 uses a handshake bus. This means that every bus transaction must be acknowledged. The DTACK input must be strobed low by the extermal circuit to indicate that the memory access has been completed successfully. (See later.)

8.5.1 68000 Memory Access Timing Diagram

Memory access for the 68000 is best explained using a timing diagram as shown below (figure 10.20).

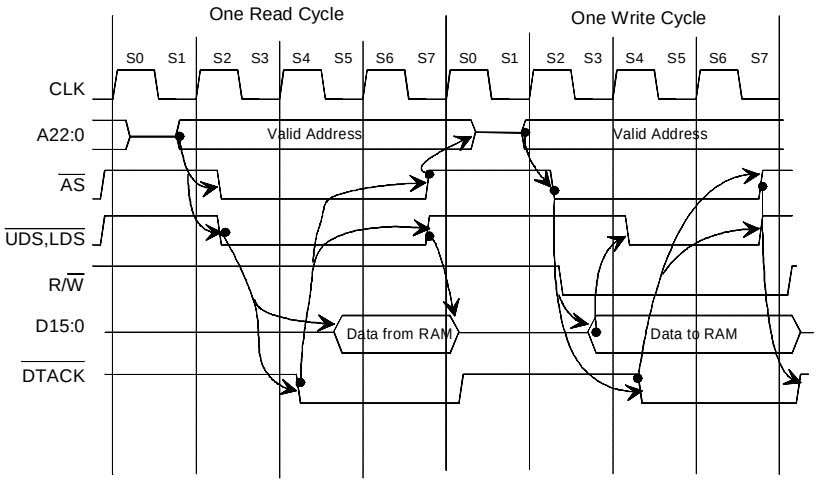


Figure 10.20 Read/Write Timing Diagram for 68000 (Simplified)

* DTACK is sampled on the falling edge of S4. If it is low, the processor proceeds to S5. If it is high, the processor insert a wait state lasting for one clock period. If DTACK is low on the falling edge of the wait state, it moves to S5, else yet another wait state is inserted.

* For the read cycle, data is read into the processor on the falling edge of S6. Assuming that no wait state is inserted, the 68000 takes 4 clock cycles (8 states) to complete a memory transaction.

* Note that the timing for a write cycle is different from that for the read cycle. During a read cycle, UDS and LDS are asserted at the same time as AS. During a write cycle, UDS and LDS comes almost a cycle later.

10.5.2 Memory Access Protocol Flowcharts

An alternative way (to timing diagram) of describing the bus transaction during memory access is to use a Protocol flowchart. Figure 10.21 shows the flowchart for a read cycle. Figure 10.22 shows that for a write cycle.

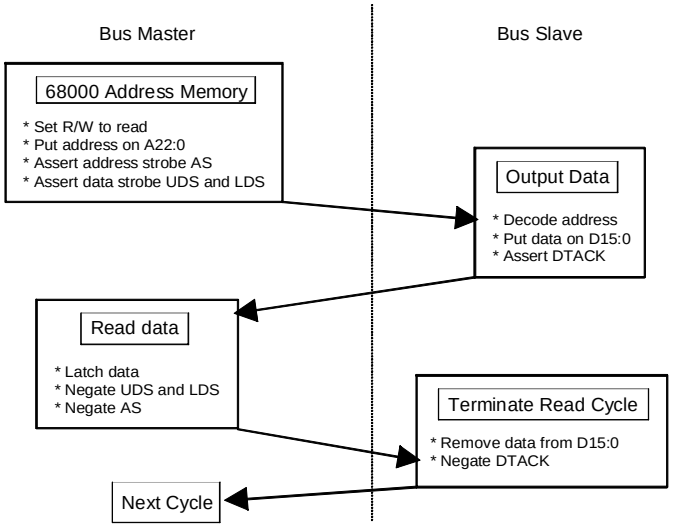


Figure 10.21 Protocol flowchart for a 68000 read cycle

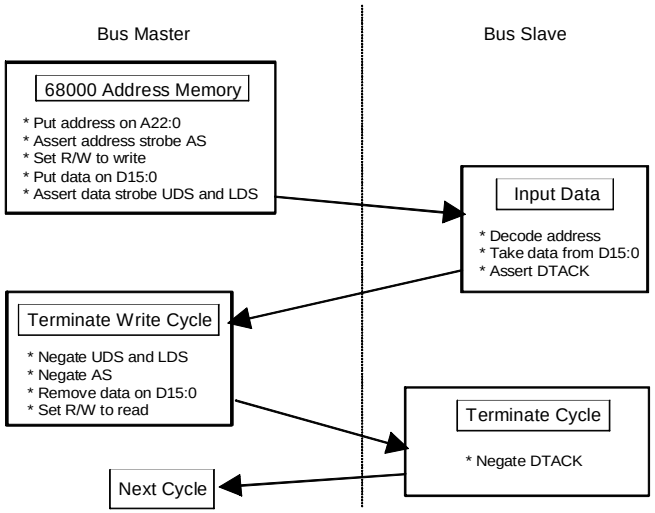
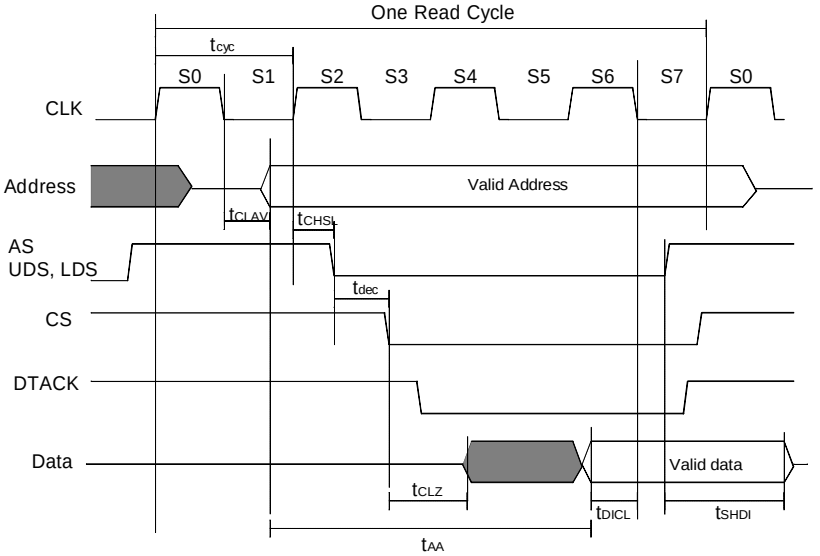


Figure 10.22 Protocol flowchart for a 68000 write cycle

The advantage of such flowcharts are that they define the sequence of event precisely. The disadvantage is that some timing information if omitted. For example, no where does it indicate that DTACK is sampled on the falling edge of S4.

Bus master is the device that drives the address and control busses. In this case, it is the 68000 processor.

10.5.3 68000 Memory Read Timing Requirements



Parameter	Symbol	Minimum	Maximum
Clock period	t_{CYC}	125	250
Clock low to address valid	t_{CLAV}	-	70
Clock high to AS, DS low	t_{CHSL}	0	60
Data in to clock low setup time	t_{DICL}	15	-
DS high to data invalid (data hold-time)	t_{SHDI}	0	-

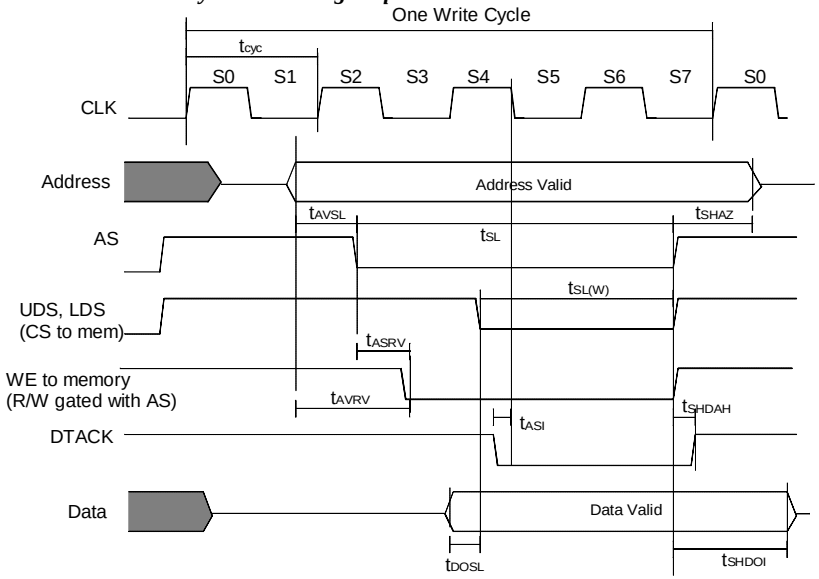
Figure 10.23 Detail Timing Diagram for a 8 MHz 68000 read cycle

Let us next consider the timing requirement imposed by this diagram on memory chips used. The important parameters are:

Meaning	Symbol	68000 Equivalent	Req. on mem.
Address access time	t_{AA}	$3t_{CYC} - t_{CLAV} - t_{DICL}$	<290
Chip deselect to output float	t_{CHZ}	t_{SHDI}	>0

It can be seen that for 8MHz 68000, the demand on memory access time is easily met. If very slow memory (such as EPROMs) are used, then wait states can easily be inserted by delaying the generation of DTACK. (We will consider such circuit later.)

8.5.4 68000 Memory Write Timing Requirements



Parameter	Symbol	Minimum	Maximum
Clock period	t_{CYC}	80	250
Address valid to AS low	t_{AVSL}	0	-
AS width low	t_{SL}	160	-
DS width low (write cycle)	$t_{SL(W)}$	80	-
AS, DS high, to address valid	t_{SHAZ}	10	-
Address valid to R/W low	t_{AVRL}	0	-
AS low to R/W valid	t_{ASRV}	-	20
Data out valid to DS low (write)	t_{DOSL}	15	-
DS high to data out invalid	t_{SHDOI}	15	-
DTACK setup time	t_{ASI}	20	-
AS, DS high to DTACK	t_{SHDAH}	0	150

Figure 10.24 Detail Timing Diagram for a 12 MHz 68000 write cycle

The write cycle timing is more complicated. Here is a extraction of the more important timing specifications for a 12 MHz 68000 (faster than that for the last table).

To see whether a memory device meets the writing timing requirement of the 68000, we need to consider a number of requirements:-

Meaning	Symbol	68000 Equivalent	Requirement
Write cycle time	t_{WC}	$t_{AVSL} + t_{SL} + t_{SHAZ}$	
Address setup time	t_{AS}	t_{AVRL}	
Address valid to end of write	t_{AW}	$t_{AVSL} + t_{SL}$	
Write pulse width	t_{WP}	$t_{SL} - t_{ASRV}$	
Data setup time	t_{DW}	$t_{DOSL} + t_{SL}$	
Data hold time	t_{DH}	t_{SHDOI}	

Again you can see that the static memory chip we considered in section 10.2.2 will meet all the requirements comfortably.

10.5.5 Wait State Insertion and Bus Error Circuits

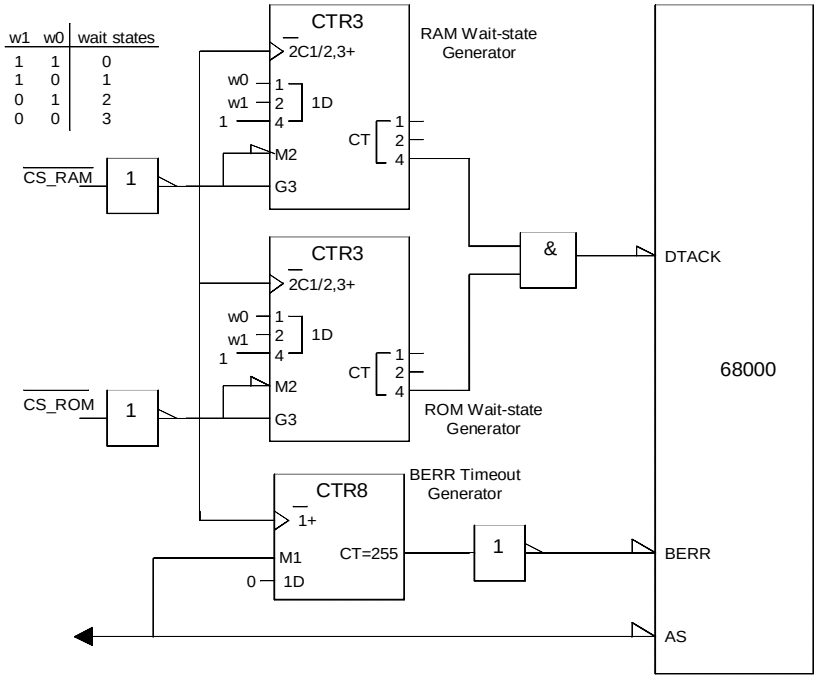


Figure 10.25 Wait state and Bus Error Generation Circuit

The circuit works like this:

- While chip select is not asserted, preload occurs on every rising clock edge and DTACK remains high. As soon as chip select is asserted, depending on the value of w1:w0, CT4 will eventually goes low, generating the acknowledge signal to DTACK. For example if w1:w0 = 11, then the counter output bit2 will go low on the next rising edge of clock and 0 wait-state will be generated. However if w1:w0=10, then the counter will count an extra clock pulse before producing the DTACK signal.
- While AS is not asserted, CTR8 is preloaded with 0. Whenever AS is asserted (low), CTR8 will start counting. If it counts up to 255 and AS remains low (meaning that it has taken 255 clock cycle to read or write!), a bus error BERR signal will be generated.

10.6 Dynamic RAM

10.6.1 Dynamic RAM cells and structure

Dynamic RAM cells has only one transistor and one parasitic capacitor:

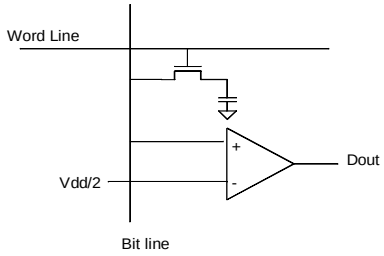


Figure 10.26 DRAM cell

The parasitic capacitor stores either a '0' or a '1' depending on the charge stored on it. This capacitor is extremely small in value, typically 32-125 x 10^{-15} Farad!
Since charge leaks away, all dynamic RAM cells need to be refreshed regularly. We will consider dynamic RAM refreshing later.

The internal structure of a DRAM chip is quite similar to that of SRAM. The memory cells are organised as a 2-D array, again with rows and columns. An entire row of cells is addressed. All cells on that row put its value on the bit line (column). At the same time, the sense amplifier is switch ON and all the cells in the row is refreshed. One of the column is then selected and routed to the output pin.

Since the column address is not needed after the sense amplifier has settled, DRAM addresses are always multiplexed - address pins are used for both row address and column address. This has two effects, it saves on number of pins, and it allow fancy ways of access the memory cells. Figure 10.27 shows a simplified block diagram of a 1Mbit DRAM chip. Currently 4M, 16M and 64M DRAM are commonly used.

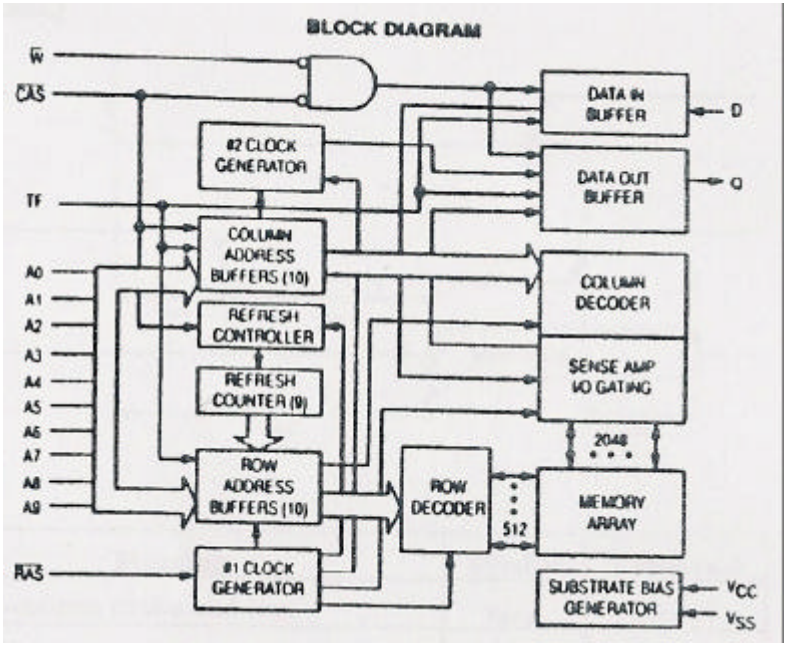


Figure 10.27 MCM511000 1Mbit DRAM block diagram

Figure 10.28 shows a simplified timing diagram for a DRAM read cycle.

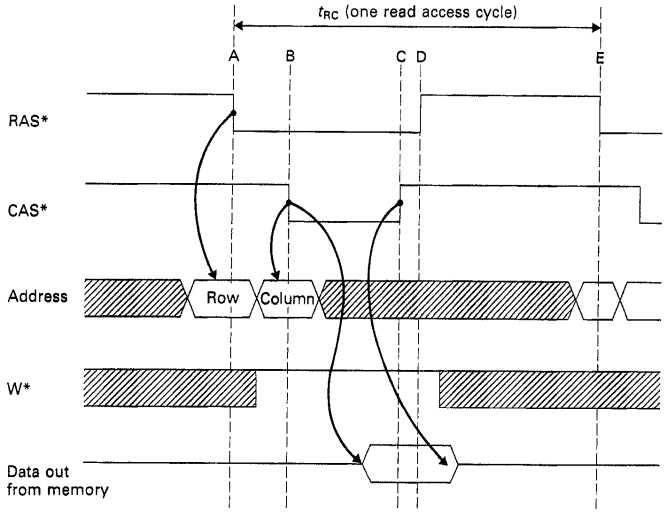


Figure 10.28 Simplified read cycle timing diagram for a DRAM

10.6.2 Dyamic RAM Timing

The following sequence of events occurs (timing information is for the above chip with 70ns access):-

A. ***RAS goes low***. The row address is latched internally and decoded. Row address setup time t_{ASR} = 0, row address hold time t_{RAH} = 10 ns.

B. ***CAS goes low*** between $t_{RCD(min)}$ = 20 nS and $t_{RCD(max)}$ = 50 ns after RAS. Column address setup time t_{ASC} = 0, column address hold time t_{CAH} = 15 ns. The write signal W and the input data (if W is low) are also read in.

B/C. ***Data output***. If W is high, the output data appears t_{RAC} = 70 ns after RAS or t_{CAC} = 20 ns after CAS whichever is later.

C. ***CAS removal***. When CAS is taken high, the output data will disappear within t_{CAC} = 20 ns.

D. ***RAS removal***. RAS can be taken high t_{RP}=50 ns after it has gone low (min RAS pulse width). It must stay high for at least t_{RC} = 130ns to give time for internal circuitries to recover.

Detail timing for DRAM is complex. We shall consider them a bit at a time.

1. Address timing

Meaning	Symbol	Value (ns)
Row-to-column strobe lead-time	t_{RCD}	20-30
Row address setup time	t_{ASR}	0 min
Row address hold time	t_{RAH}	10 min
Column address setup time	t_{ASC}	0 min
Column address hold time	t_{CAH}	15 min

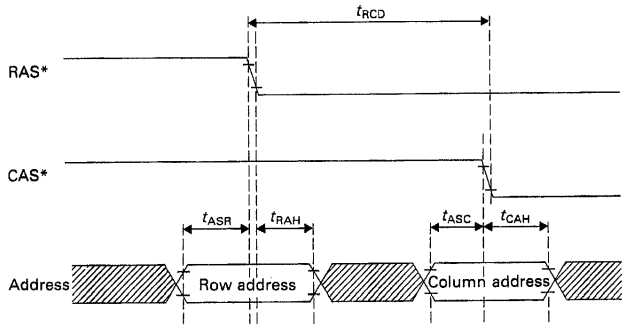
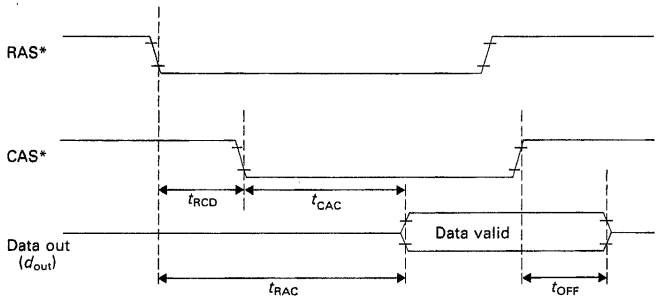


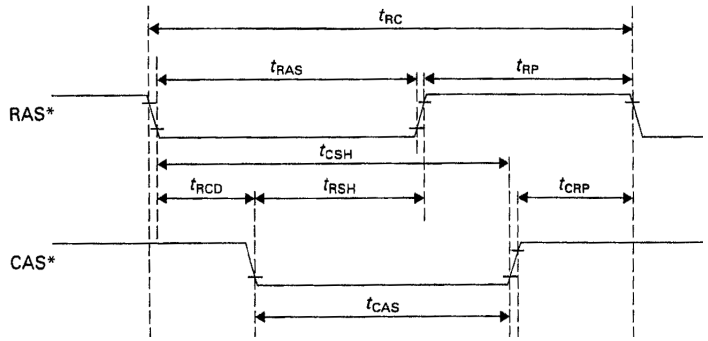
Figure 10.29 Address Timing Details

2. Data Timing



Meaning	Symbol	Value (ns)
Row-to-column strobe lead-time	t_{RCD}	20 - 50
Access time from column address strobe	t_{CAC}	20 max
Access time from row address strobe	t_{RAC}	70 max
Output buffer turn-off time	t_{OFF}	0 -20

3. RAS and CAS Timing



Meaning	Symbol	Value (ns)
Random access cycle time	t_{RC}	130 min
Row address strobe pulse width	t_{RAS}	70 - 10,000
Row address strobe precharge time	t_{RP}	50 min
CAS hold time	t_{CSH}	70 min
Row-to-column strobe lead-time	t_{RCD}	20 - 50
RAS hold time	t_{RSH}	20 min
Column address strobe pulse width	t_{CAS}	20 - 10,000
Column-to-row strobe precharge time	t_{CRP}	-5 min

10.6.3 Design Example 4: DRAM Interface with 68000

In addition to address decoding, DRAM interface requires two addition circuits for:

a) Row-column address multiplexing
b) Memory refresh

Figure 8.32 shows a simplified diagram for a 68000 DRAM interface circuit. We are assuming here that 1M x 1 DRAM chips are used. We need 16 chips organised as two banks of eight.

* We will first consider (a) and its associated control signal generation.
* The first multiplex selects either the row or the column address to be sent to the DRAM. It is advantageous to use upper bits for row address and lower bits for column address (reason will be clear later).
* The second multiplexer selects whether a normal memory access is made, or whether it is a memory refresh operation. (We will consider refresh later.)
* The address decoder provide the DRAMSEL signal which would be to generate RAS and CAS signals.
* The Timing Control circuit is the heart of the DRAM controller. It has to provide all the relevant signals to the banks of DRAM and the MUXs.

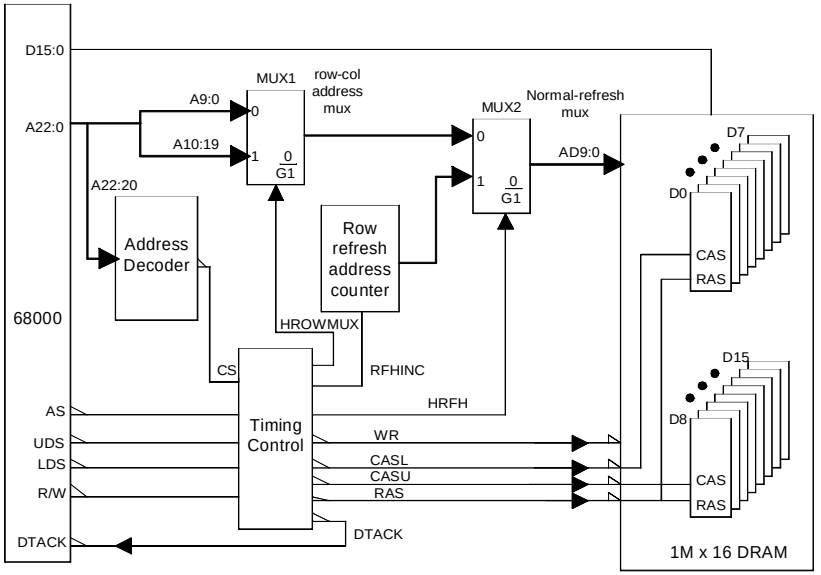


Figure 10.32 Overall Structure of a 68000 DRAM Interface Circuit

The signals to be generated need to obey the following timing requirements:-

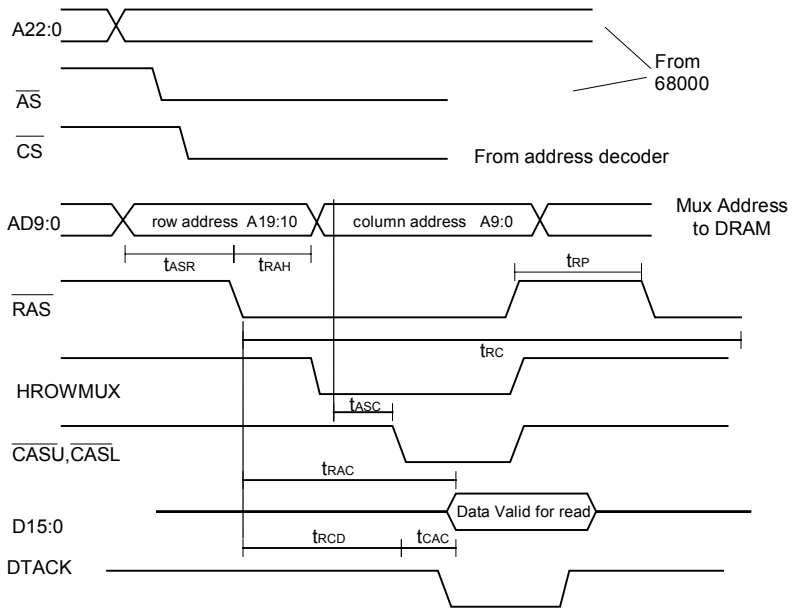


Figure 10.33 Essential DRAM timing for 68000 interface

The few important timing parameters are:-

- row address setup, hold times and column address setup time: t_{ASR}, t_{RAH}, t_{ASC}
- read cycle time and row address precharge time: t_{RC}, t_{RP}
- data valid time after row and col address strobes: t_{RAC}, t_{CAC}
- row-to-column strobe delay: t_{RCD}

The timing requirements imposed by a 1Mbit DRAM is given on pages 91, 92.

The above timing diagram suggests that the $\overline{RAS}$, HROWMUX and $\overline{CAS}$ signals are essentially delayed versions of the CS signal. It suggests immediately that a shift register might be used to generate most of the signals.

Ignoring memory refresh circuits, the following circuit will provide all the necessary signals (figure 10.34). We are assuming 70ns 1Mbyte RAMs are used.

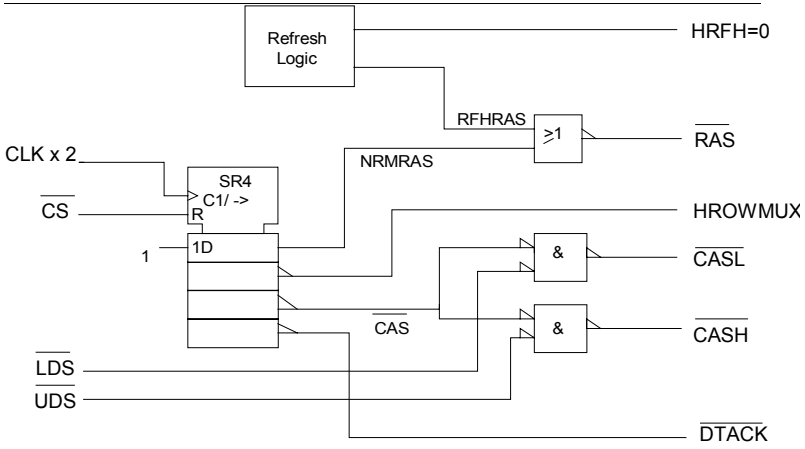


Figure 10.34 Timing Control Circuit for DRAM interface

The timing diagram for this circuit is (figure 10.35):

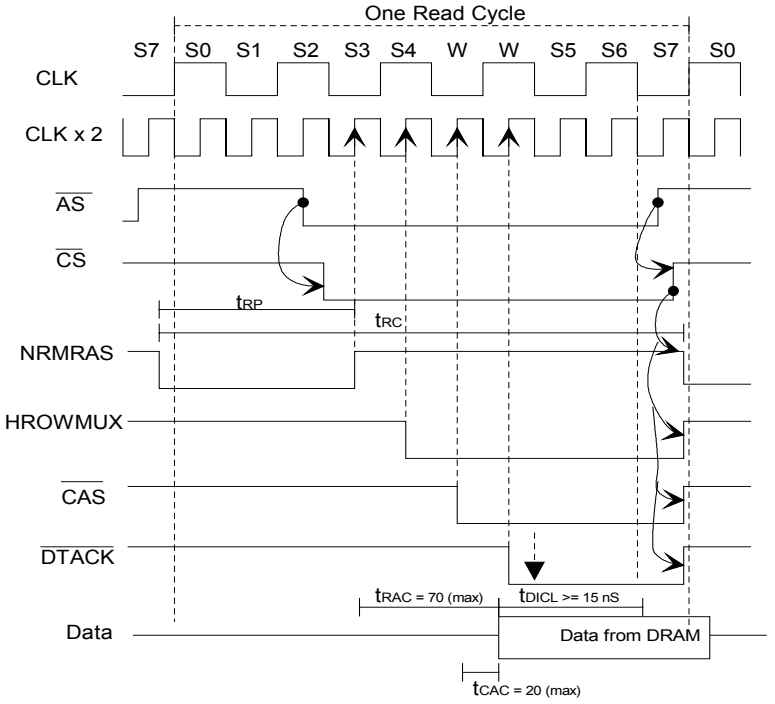


Figure 10.35 Timing Diagram for the DRAM Interface Circuit

If the wait-state is not required, it can easily be eliminated if the HROWMUX signal is also used to drive DTACK. Then the falling edge of S4 will sample a low DTACK, thus generating 0 wait state.

10.6.4 Dynamic Memory Refresh

All dynamic memory need refreshing. A refresh is effect by accessing every row within the memory chip. All rows within the chip must be accessed during a fixed duration. For 1Mbit DRAM, this refresh period is 8 ms.

The 1Mbit DRAM contains 1024 row x 1024 column. However, the memory matrix is actually organised as two blocks of 512 rows each. Each time a refresh cycle is initiated, two rows (one from each block) of cells are refreshed together. In other word, every refresh cycle will refresh 2048 column locations.

The following table shows the frequency of refresh, number of refresh cycles as a function of memory capacity:

Capacity	Refresh period (ms)	Refresh Cycles
256K	4	256
1M	8	512
4M	16	1024
16M	*32 - 64*	*1024 - 2048*

Therefore, on average one refresh cycle is need every 15.6 μs disregard which memory chip is used. Refresh can be performed in either a single burst of 512 consecutive refresh cycles (for 1M chips) every 8 milliseconds, or distributed over time with one every 15.6 μs, or somewhere in between. Each refresh cycle takes a minimum of t_{RC} (read cycle time) to complete. This is (typically) 130 ns minimum for a 1M DRAM. Therefore refreshing use up no more than 1% of processing time.

DRAM chips provide three possible refresh method:

1. RAS only refresh
2. CAS before RAS refresh
3. Hidden refresh

RAS only refresh (Figure 10.36)

- This is performed by supplying row addresses A8:0 and completing a RAS cycle (t_{RC}).
- RAS must be asserted for a minimum duration of t_{RAS}, and negated for at least t_{RP}.

- A9 is ignored during RAS only refresh (because A9 is usually used to select which block to address. During refresh, both blocks are accessed together.)
- CAS must be held high during the entire refresh cycle.
- An external row counter (9-bits) must be used to supply the row address.

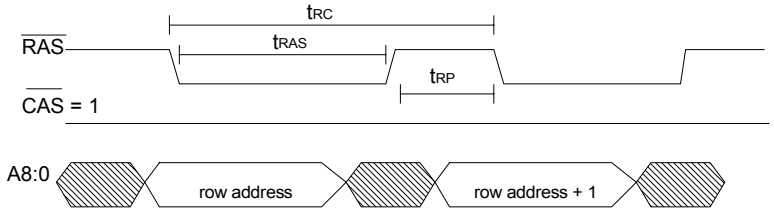


Figure 10.36 RAS only refresh timing

CAS before RAS refresh (Figure 10.37)

- This reverses the order of CAS and RAS signals: CAS is asserted before RAS.
- This activate an internal row counter to generate the refresh row address. External address on the bus is ignored during this cycle.

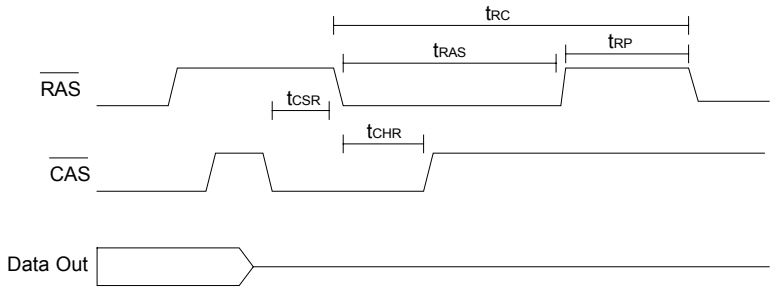


Figure 10.37 CAS before RAS refresh

Hidden Refresh (Figure 3.38)

- Hidden refresh is initiated with a normal memory access cycle.
- At the end of the cycle, CAS is held asserted (instead of returning to high) while RAS is return high to complete the cycle.
- When RAS goes low again, an internal hidden refresh is performed. The refresh row counter is used to address a row.
- While refresh is taking place, the valid data is held on the bus for the processor to read. This is particular valuable since most modern processors run faster than DRAMs, data is often needed for longer than one cycle.

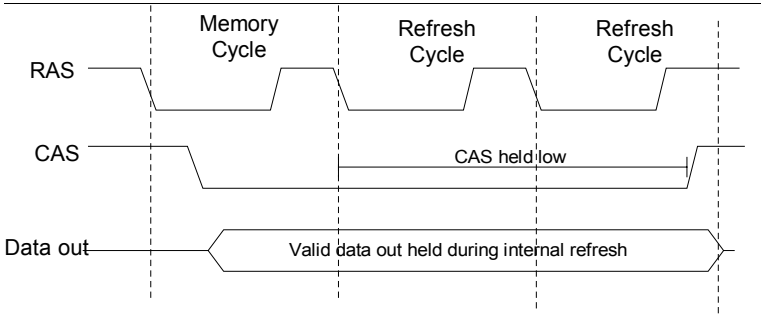


Figure 10.38 Hidden Refresh

10.6.5 Design Example5: DRAM Refresh with 68000

Let us consider the circuit needed to refresh DRAM on a 68000 system using the normal RAS only refresh. In order not to hold up the processor for long durations, we will carry out 512 refresh cycles in bursts of 8 cycles. Therefore we need to perform 64 bursts in 8 ms. The refresh clock is therefore 8KHz.

During refresh, the microprocessor must be prevented from accessing memory. This is achieved by using the bus arbitration signals: bus request (BR), bus-grant (BG) and bus grant acknowledge (BGACK). The way these arbitration signal work is depicted in figure 10.39 & 10.40. The DRAM refresh circuit asserts BR. After the processor finishes its current cycle, it floats the bus and surrenders it to the DRAM control circuit. It indicates this by asserting the BG signal. DRAM refresh circuit then asserts BGACK signal while it is controlling the bus. When it relinquishes control of the bus back to the 68000, BGACK is negated.

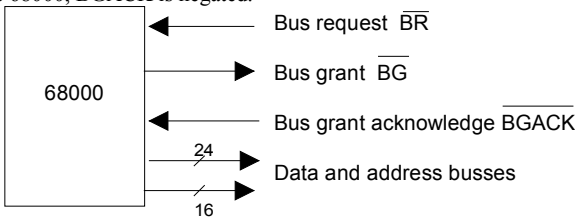


Figure 10.39 Bus arbitration signals for 68000

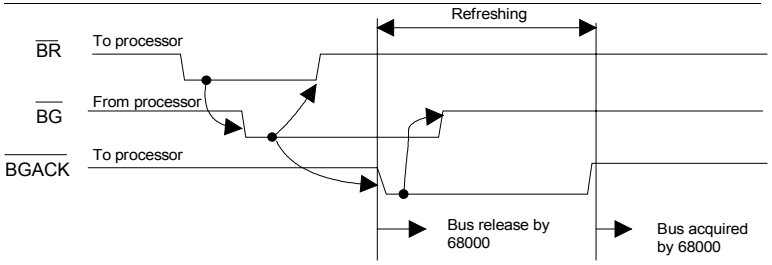


Figure 10.40 Bus arbitration timing for 68000

The block diagram for the refresh circuit is shown in figure 10.41. The refresh counter provides two addresses: a 3-bit address to cycle through the burst of 8 row addresses, and a 6-bit address giving the burst number. Together they make the 9-bit row address needed for freshing. Before designing the actual circuit, we must first draw the timing diagram (figure 10.42):

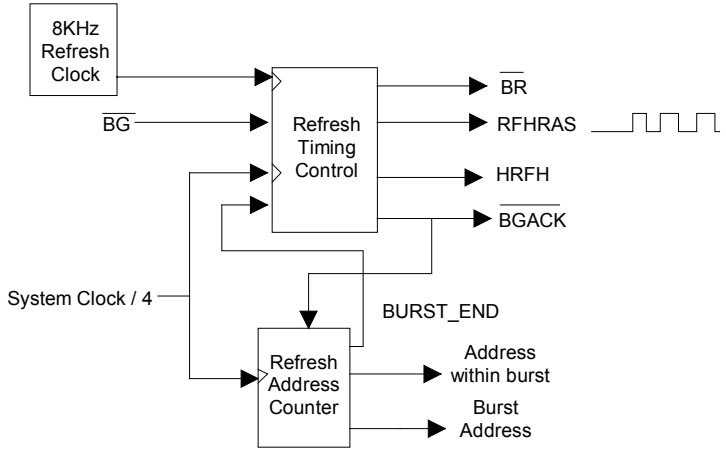


Figure 10.41 Block diagram of the DRAM refresh circuit

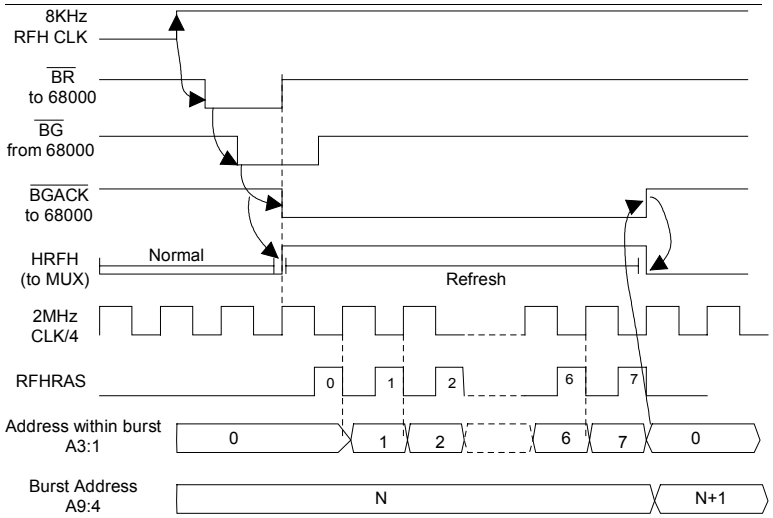


Figure 10.41 DRAM 8 cycle Burst Refreshing Timing Diagram

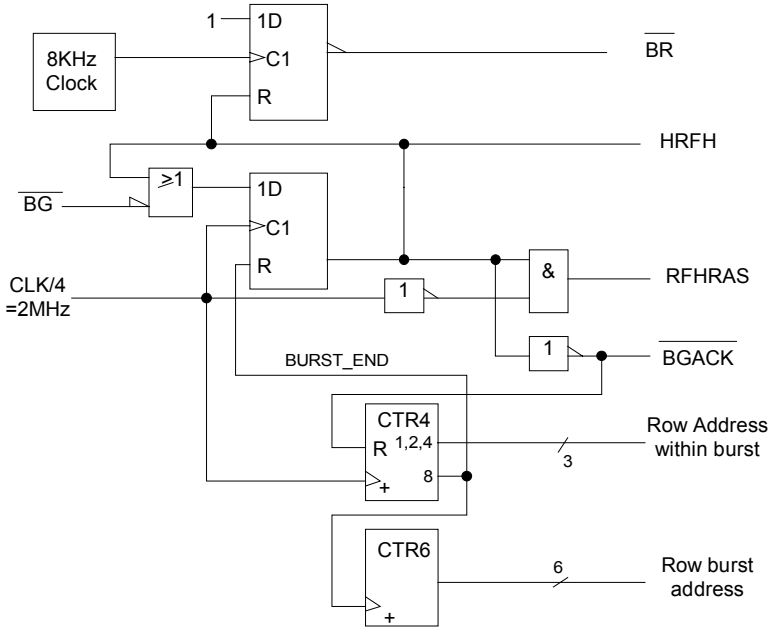


Figure 10.43 DRAM Refresh Control Circuit for 68000

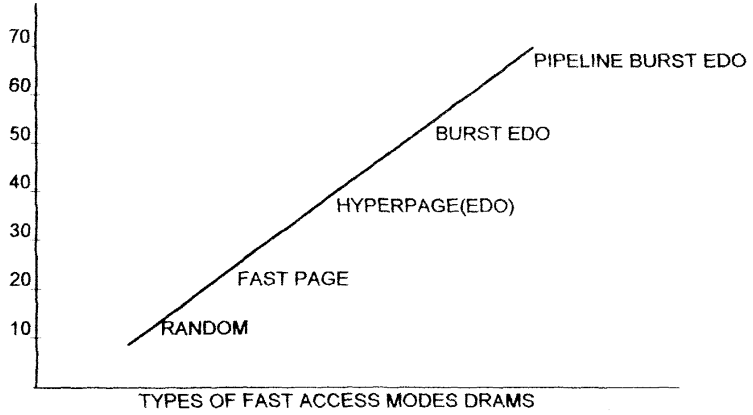
Figure 10.43 shows an implementation of the refresh control circuit. Notes the following features:

- The positive edge of the 8 KHz refresh clock initiates the refresh burst sequence. This generates a bus request (BR) to the 68000 by setting the first D flip-flop.
- The second D flip-flop is set when the bus grant (BG) is returned by the 68000. It also resets the first flip-flop.
- The HRFH signal is gated with the inverted 2 MHz clock signal. Note that the refresh clock control should be 1/4 of system clock. (Each basic read cycle takes 4 system clock cycles.)
- The BGACK signal is simply the inverted version of HRFH. It is used to enable the 9 bit row address counter.
- The row address counter is organised as two cascaded ripple clock counters. The first provides the address within a burst (3-bit). The second generates the remaining 6 bit address.

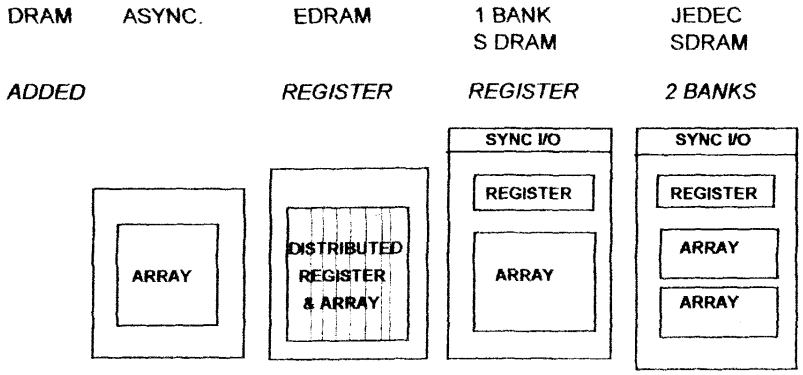
This circuit is efficient in that it takes very few gates to implement. However, the same problem could be solved using a finite state machine. Although this would likely be a larger circuit, the design methodology is well defined.

10.7 Synchronous DRAM

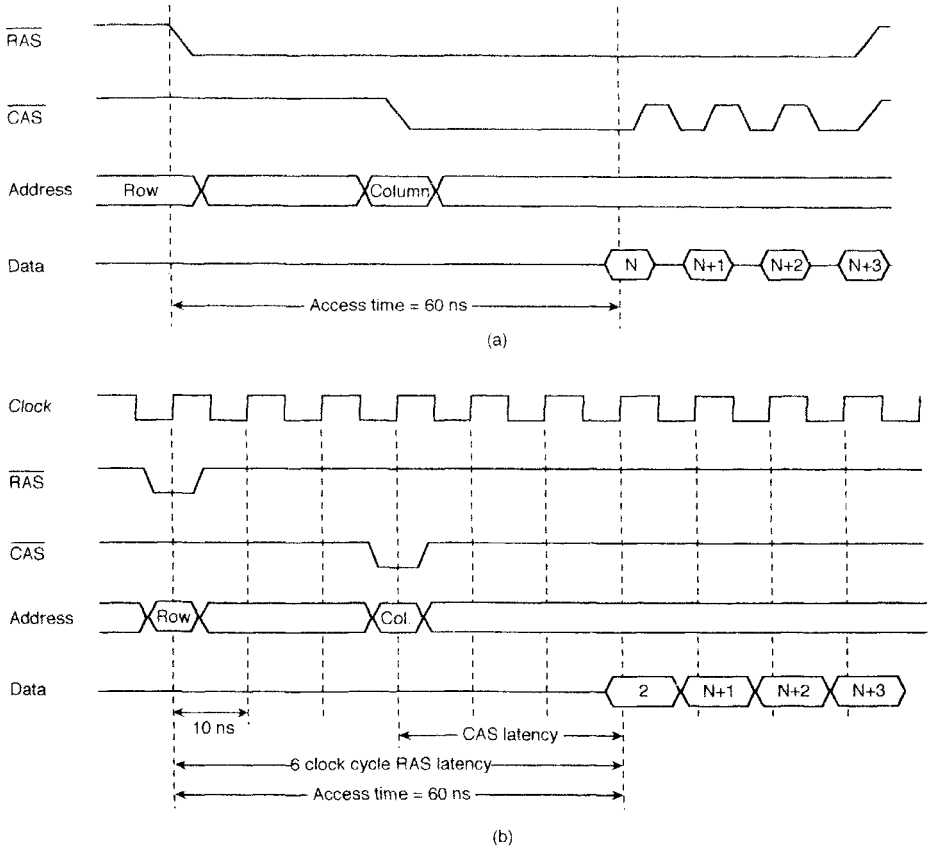
Asynchronous DRAM speed has not really increased much over years. See diagram below:



Synchronous DRAM is now the standard method of interfacing to RAM. Essentially it exploits the page mode feature of asynchronous DRAM and add synchronous registers and I/O out the outside:



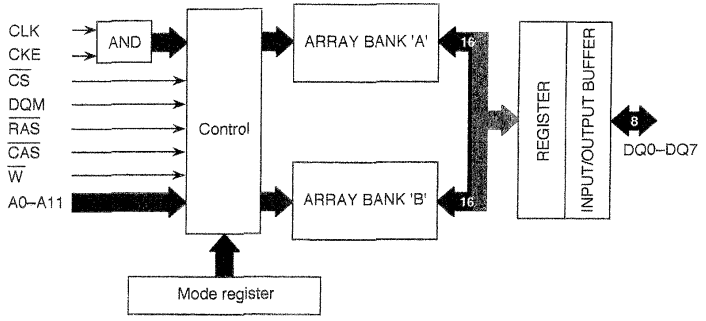
Here is a comparison of DRAM with asynchronous and synchronous control. For synchronous DRAM (SDRAM), row and column addresses do not need to stay on the bus. Once latched, the address and data bus are free for the microprocessor to do other things. After some latencies, data starts streaming out.



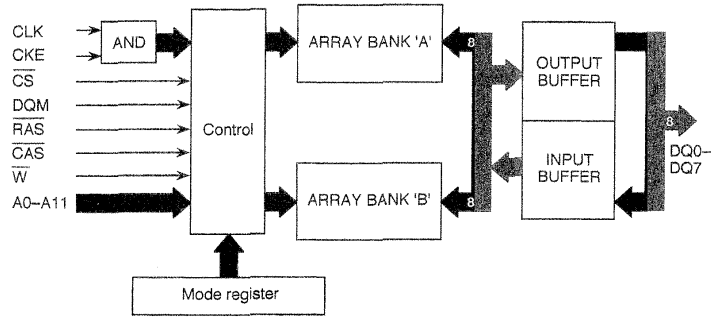
Here is a summary of features found in a 16M JEDEC type SDRAM:

- Fully synchronous with all signals referenced to a positive clock edge.
- Organization: dual internal banks, ×4, ×8, ×9, ×16, ×18
- Package: 400 mil, 0.8 mm, 50-pin TSOPII (JEDEC Standard)
- Power supply: 3.3 V, 10%
- Interface: LVTTL
- Programmable burst length: 2, 4, or 8
- Programmable output sequence: serial or interleaved
- Control pins: Chip Select and Clock Enable
- DQ Mask Function
- Byte control using LDQM/UDQM on ×16, ×18 option
- Programmable read latency from column address
- CBR auto refresh
- Self refresh during power down
- Pulsed RAS
- Random Column Address on alternate cycles during burst
- Random

SDRAM can have two types of output structures: with multiple word output registers (called "prefetch type") and without such output ("pipeline type"). These are shown in the figure below:-

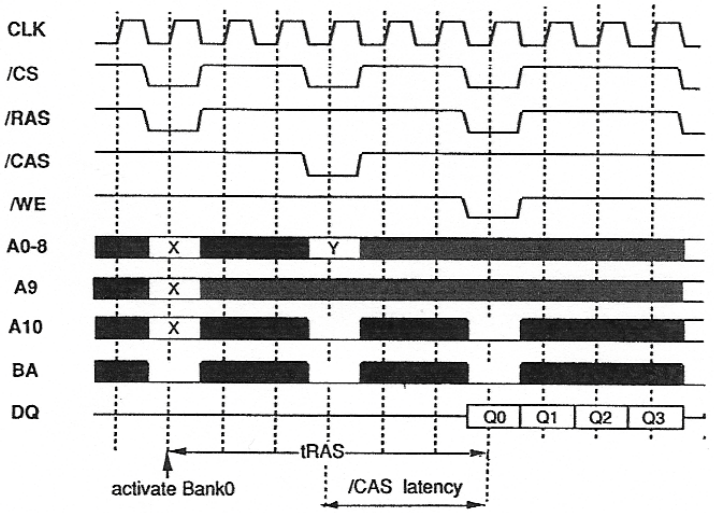


Prefetch output structure



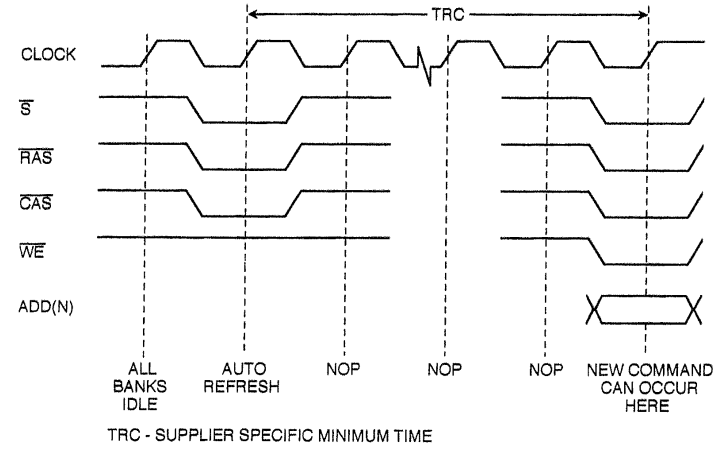
Pipeline type output structure

The following timing diagram shows the read cycle timing for a SDRAM (source: Mitsubishi). Note the RAS\ and CAS\ latency.



RAS and CAS latency in SDRAM read cycle

The CAS\ latency of the first address in aburst can be specified as 1, 2, or 3 clock cycles. This latency value is programmed in the mode register of the SDRAM.



TRC - SUPPLIER SPECIFIC MINIMUM TIME

SDRAM also has a "self refresh" mode defined during which the device will refresh itself without external circuit. The figure below shows the timing diagram during self refresh. To enter self refresh CS\, RAS\ , CAS\ must be asserted (low) and WE\ must be high.