

Real-time Digital Signal Processing with the TMS320C6000

Objectives:

- ◆ Learn the architecture of a typical DSP
- ◆ Learn how to perform basic real-time DSP tasks on 'real' hardware
- ◆ Learn about interrupts and I/O devices

Course Information

Lecturers

Mike Brookes, Peter Cheung, Darren Ward

Web page

http://www.ee.ic.ac.uk/pcheung/teaching/ee3_Study_Project/index.html

Assessment

Test (14 June) 25%,

Labs (22 June) 30%, Project (22 June) 45%

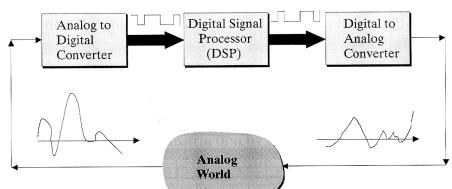
Deliverables

1. Labs 3-4,6-8: Program listings (with comments) with evidence that programs work
2. Project: Full listing of your program with a short description (2-9) pages and assessment of performance

You will be working in pairs, each pair submits a single set of reports

Digital Signal Processing

- ◆ Digital signal processing involves the manipulation of digital signals to extract useful information from them.



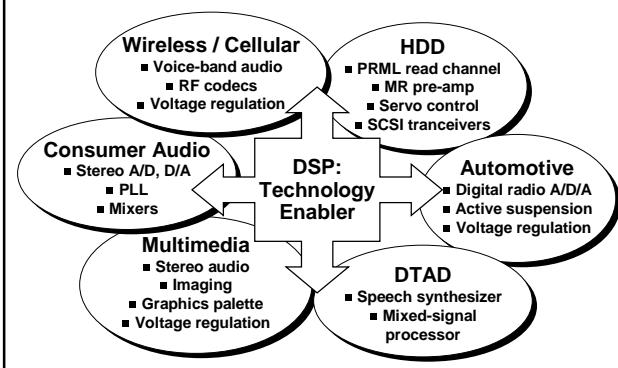
DSP vs VLSI

- ◆ DSPs have more application flexibility
- ◆ DSPs are more cost effective; VLSI are normally built for a single application / customer
- ◆ Higher sampling rates can typically be achieved using VLSI
- ◆ New features (bug fixes) can be added to DSP with software upgrade

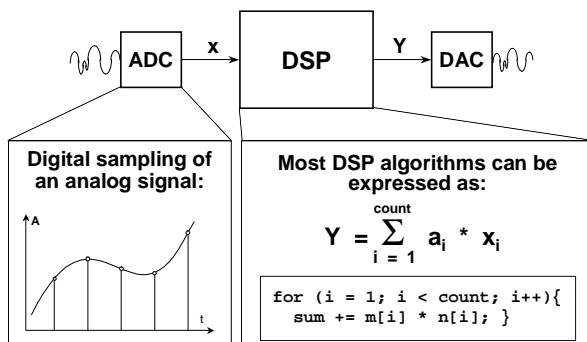
DSP vs Microprocessor

- ◆ DSPs can do several memory accesses in a single instruction
- ◆ DSPs are optimized to handle repetition / looping operations common in signal processing algorithms
- ◆ DSPs allow specialized addressing modes (e.g., circular, indirect) to implement SP algorithms
- ◆ DSPs possess peripherals that allow for efficient I/O interfacing

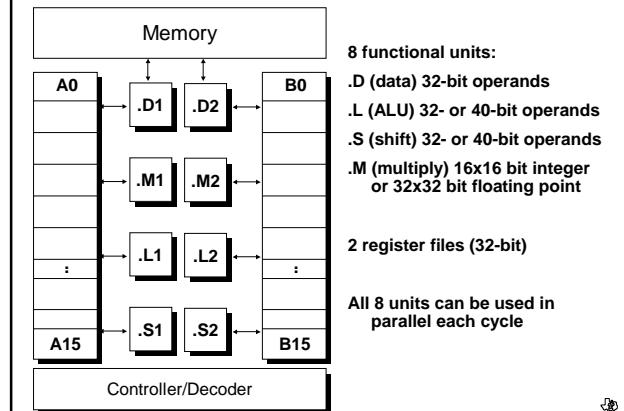
Present Day Applications



What Problem Are We Trying To Solve?



C6000 Architecture



6000 Series Devices

Device	MIPS	MHz	KBytes	Pins	W	\$	Periphs
6201	1600	200	128	352	1.3	80 - 100	D2H
6202	2000	250	384	384/352	2.1	110 - 170	D3X
6203	2400	300	896	384	1.3	150 - 190	D3X
6204	1600	200	128	384	0.8	30 - 60	D2X
6205	1600	200	128	306	0.8	40 - 70	D2P
6211	1200	150	72	256	0.9	25 - 40	E2H

Device	MFLOPS	MHz	KBytes	Pins	W	\$	Periphs
6701	1000	167	128	352	1.4	110 - 170	D2H
6711	900	150	72	256	1.1	25 - 50	E2H
6712	600	100	72	256	0.7	10 - 22	E2

Peripherals Legend:

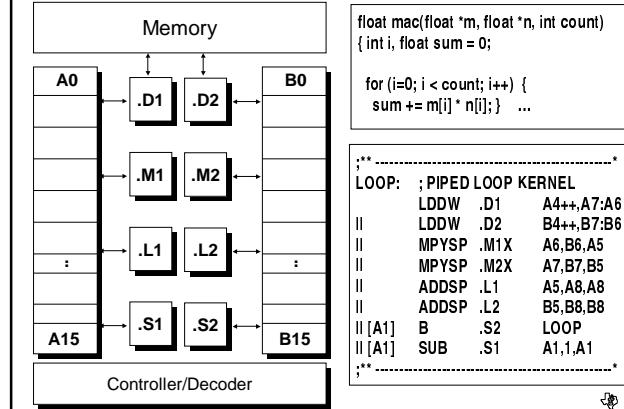
D,E DMA (4), EDMA (16)
2,3 # of McBSP Serial Ports

H,X,P HPI (Host Port), XBUS, PCI

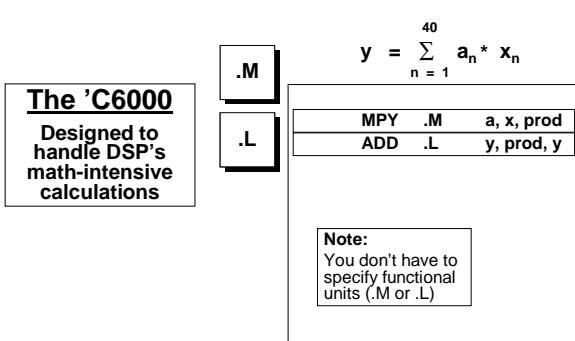
Pin-for-Pin Compatibility:

6201 & 6701
6211 & 6711 & 6712
6202 & 6203 & 6204

Fast MAC using Natural C

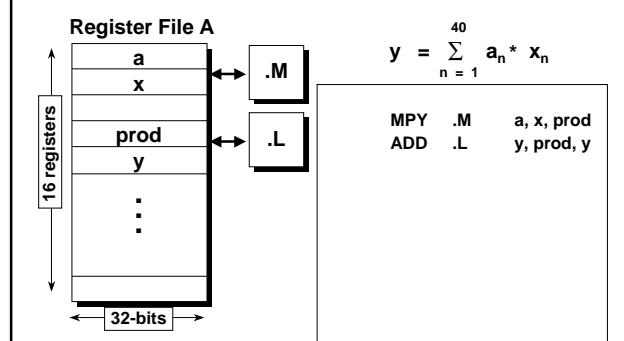


The Core of DSP : Sum of Products



Where are the variables?

Working Variables : The Register File



How are the number of iterations specified?

Loops: Coding on a RISC Processor

1. **Program flow:** the branch instruction

```
B      loop
```

2. **Initialization:** setting the loop count

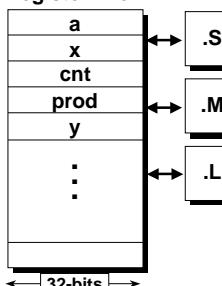
```
MVK 40, cnt
```

3. **Decrement:** subtract 1 from the loop counter

```
SUB  cnt, 1, cnt
```

The “S” Unit : For Standard Operations

Register File A



$$y = \sum_{n=1}^{40} a_n * x_n$$

```
loop:
    MVK .S 40, cnt
    MPY .M a, x, prod
    ADD .L y, prod, y
    SUB .L cnt, 1, cnt
    B .S loop
```

How is the loop terminated?

Conditional Instruction Execution

To minimize branching, **all** instructions are conditional

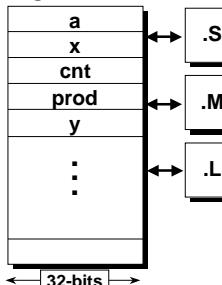
```
[condition] B loop
```

Execution based on [zero/non-zero] value of specified variable

Code Syntax	Execute if:
[cnt]	cnt ≠ 0
[!cnt]	cnt = 0

Loop Control via Conditional Branch

Register File A

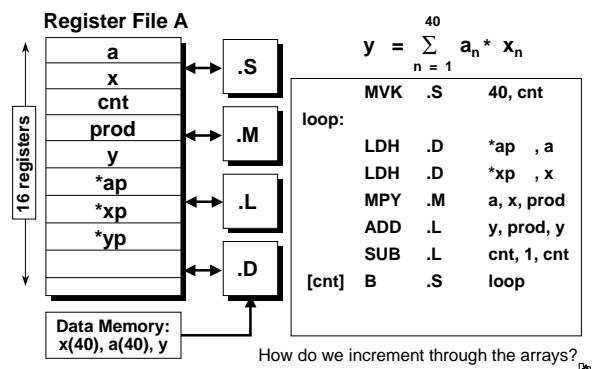


$$y = \sum_{n=1}^{40} a_n * x_n$$

```
loop:
    MVK .S 40, cnt
    MPY .M a, x, prod
    ADD .L y, prod, y
    SUB .L cnt, 1, cnt
    [cnt] B .S loop
```

How are the a and x array values brought in from memory?

Memory Access via “.D” Unit

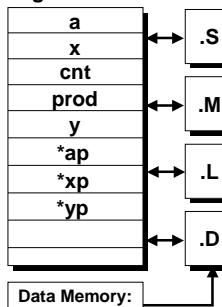


$$y = \sum_{n=1}^{40} a_n * x_n$$

```
loop:
    LDH .D *ap, a
    LDH .D *xp, x
    MPY .M a, x, prod
    ADD .L y, prod, y
    SUB .L cnt, 1, cnt
    [cnt] B .S loop
```

Auto-Increment of Pointers

Register File A



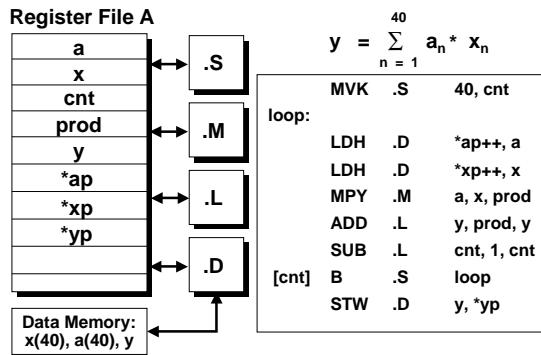
$$y = \sum_{n=1}^{40} a_n * x_n$$

```
loop:
    LDH .D *ap++, a
    LDH .D *xp++, x
    MPY .M a, x, prod
    ADD .L y, prod, y
    SUB .L cnt, 1, cnt
    [cnt] B .S loop
```

How do we store results back to memory?

Data Memory: x(40), a(40), y

Storing Results Back to Memory

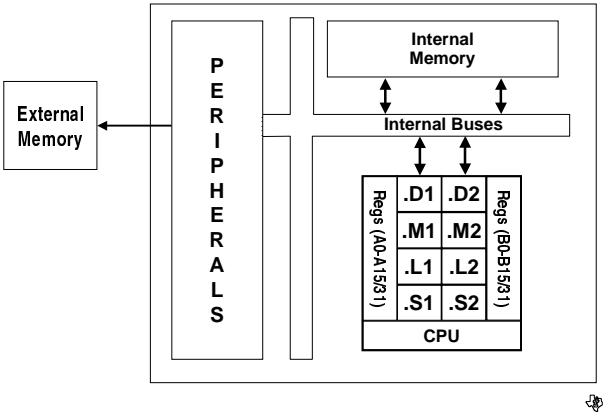


'C6700 : RISC-like instruction set

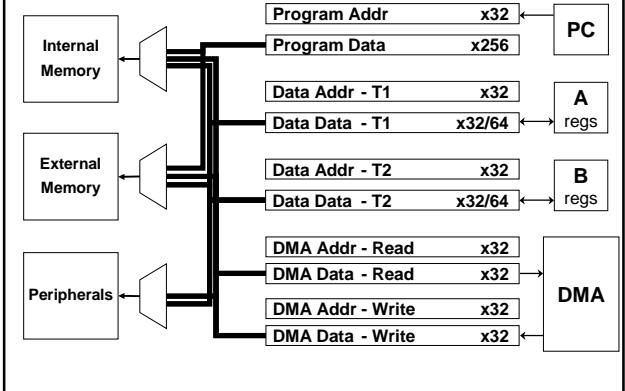
.S Unit			.L Unit		
ADD	NEG	ABSSP	ABS	NOT	ADDSP
ADDK	OR	ABSDP	ADD	SADD	ADDDP
ADD2	SET	CMPGTSP	AND	SAT	SUBSP
AND	SHL	CMPLETP	CMPEQ	SSUB	SUBDP
B	SHR	CMPGTD	CMPLT	SUBC	INTSP
CLR	SSHLL	CMPEQD	CMPLT	XOR	INTDP
EXT	SUB	CMPLTDP	LMBD	ZERO	SPINT
MV	XOR	RCPS	MV	NORM	SPRTUNC
MVC	ZERO	RCPD	NEG		DPS
MVK		RSQRSP			
MVKH		RSQRDP			
		SPDP			

.M Unit		
MPY	SMPY	MPYSP
MPYH	SMPYH	MPYDP
MPYLH		MPYI
MPYHL		MPYID
No Unit Used		
NOP		IDLE

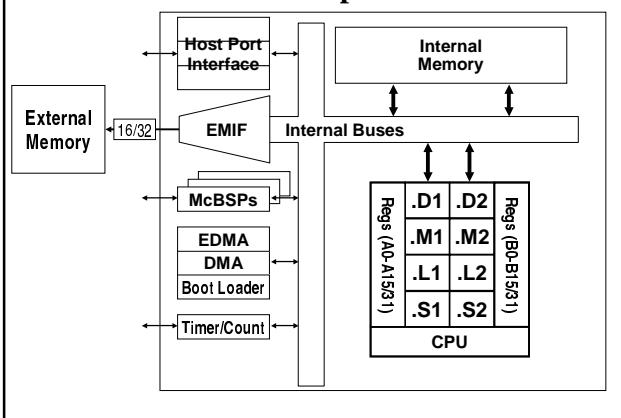
'C6000 System Block Diagram



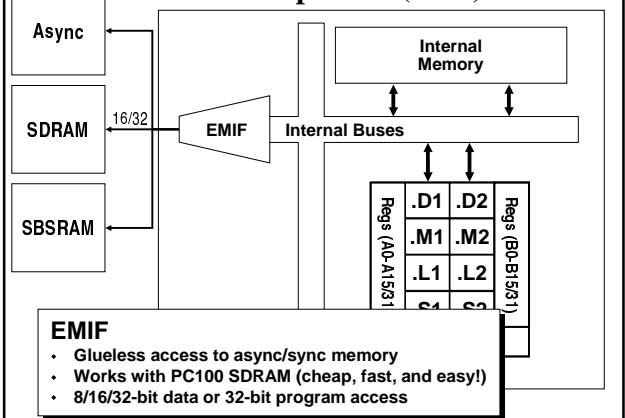
'C6000 Internal Buses

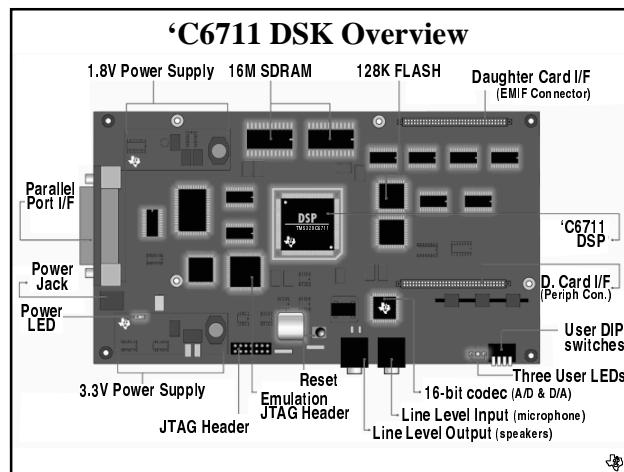
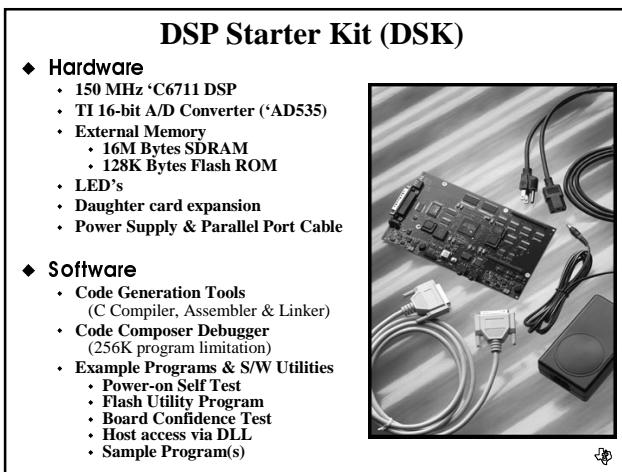
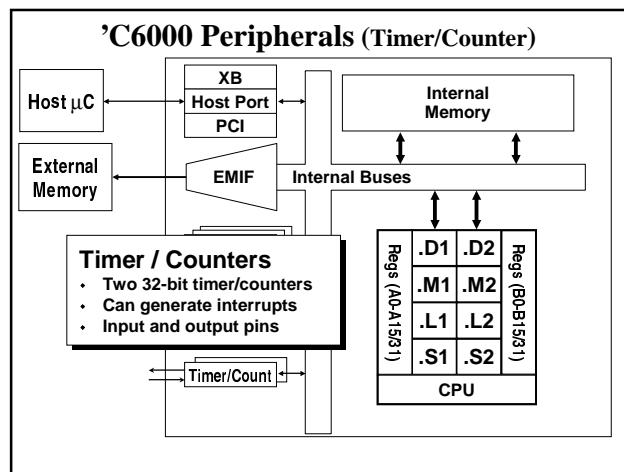
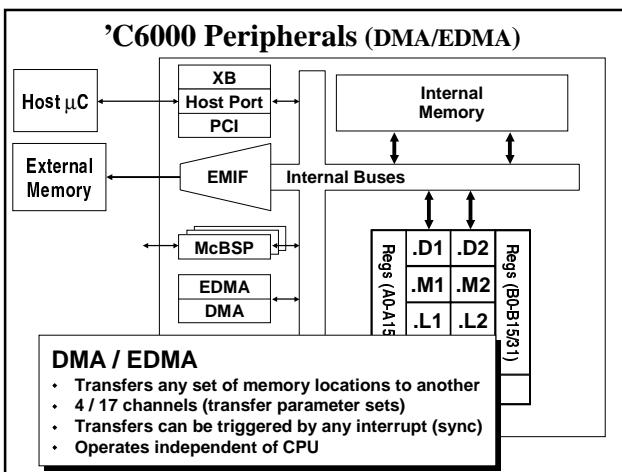
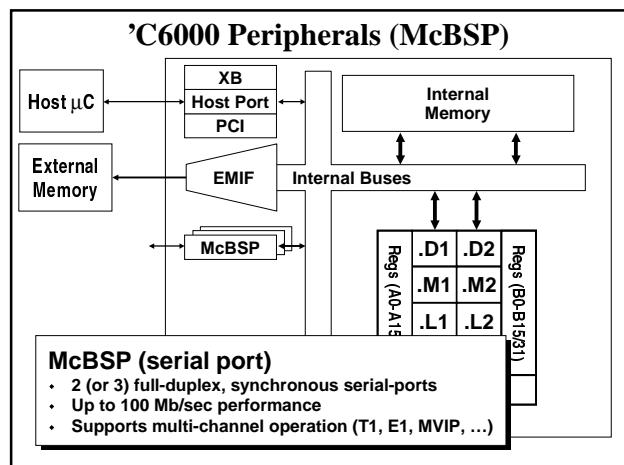
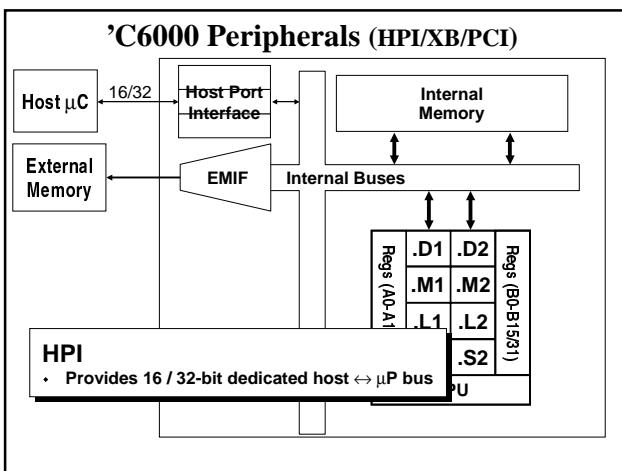


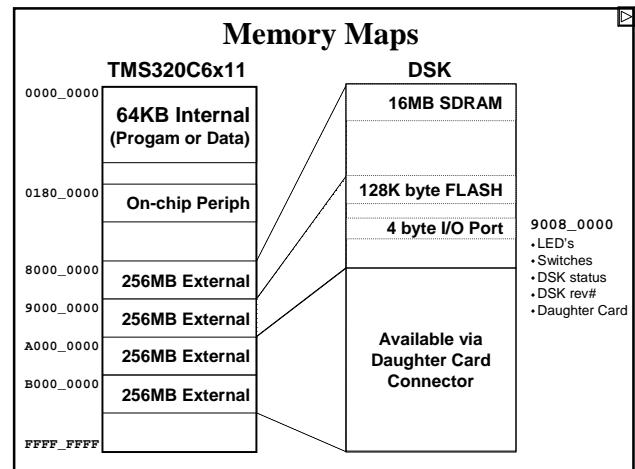
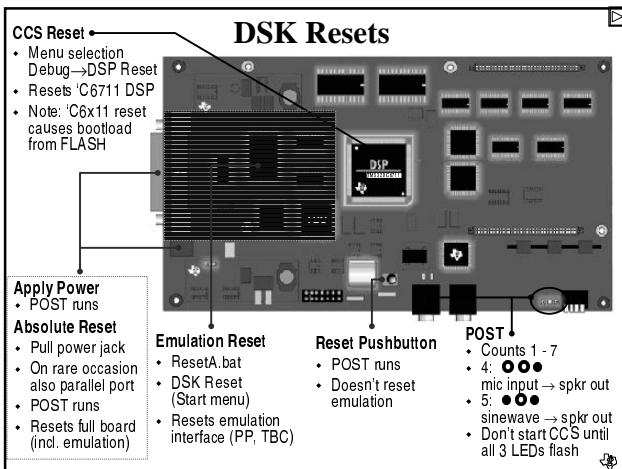
'C6000 Peripherals



'C6000 Peripherals (EMIF)







Win32 API for Host

dsk6x_open()	Open a connection to the DSK
dsk6x_close()	Close a connection to the DSK
dsk6x_reset_board()	Reset the entire DSK board
dsk6x_reset_dsp()	Reset only the DSP on the DSK
dsk6x_coff_load()	Load a COFF image to DSP memory
dsk6x_hpi_open()	Open the HPI for the DSP
dsk6x_hpi_close()	Close the HPI for the DSP
dsk6x_hpi_read()	Read DSP memory via the HPI
dsk6x_hpi_write()	Write to DSP memory via the HPI
dsk6x_generate_int()	Generate a DSP interrupt

