Topic 11
Pass Transistor Logic

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Reading: "Top-Down Pass-Transistor Logic Design", K. Yano etc., IEEE J. of Solid-State Circuits, Vol 31, No. 6, June 1996.

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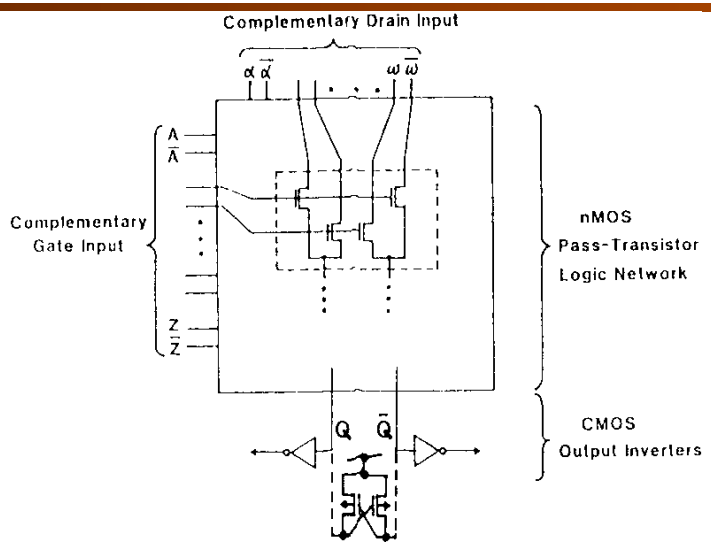
Recent development in PTL

- New development by designers at Hitachi Japan in the last 10 years.
- Three circuit styles proposed:
  - ➢Complementary Pass-transistor Logic (CPL), 1990
  - ➢Double Pass-transistor Logic (DPL), 1993
  - ➢Lean Integration with Pass-transistors (LEAP), 1996
- All exploit pass-transistors to implement general logic functions

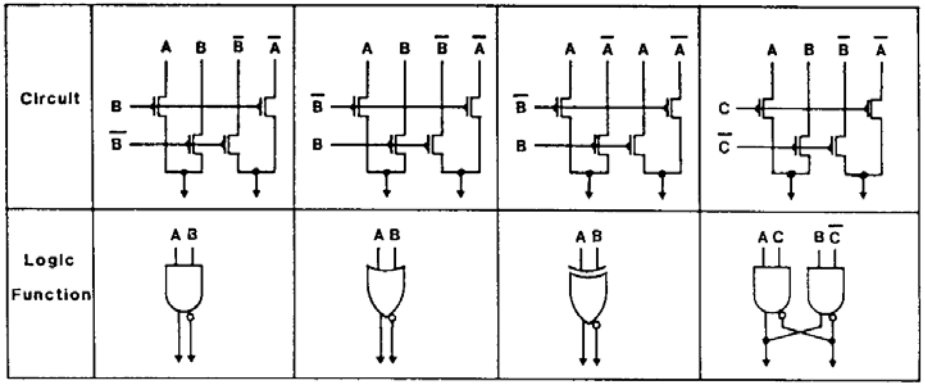
Complementary Pass-transistor Logic (CPL)

- "A 3.8 ns CMOS 16 x 16b Multiplier Using Complementary Pass -Transistor Logic" by K. Yano etc., IEEE J. of Solid-state Circuits, Vol 15, No 2, April 1990.
- Logic network employs input signals at both gate and drain terminals.
- Inputs and Outputs are always complementary.
- Outputs from network provide strong '0's but weak '1's. Inverters and PMOS pull-ups provide amplification and buffering as necessary.

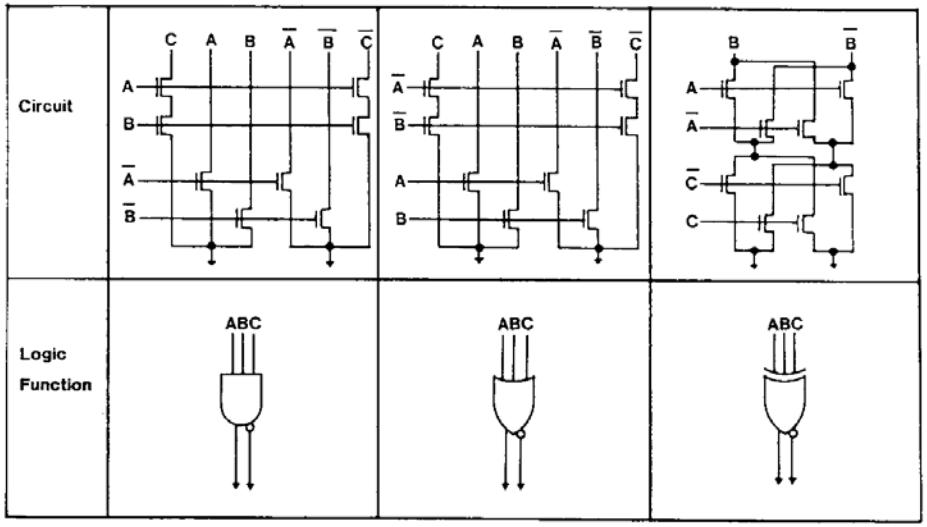
Complementary Pass-transistor Logic (CPL)



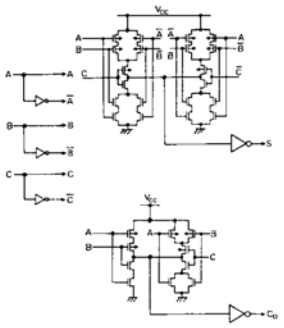
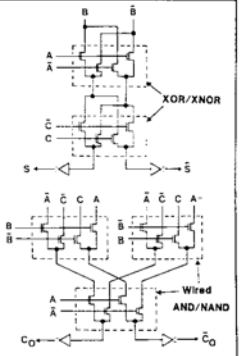
Basic gates designed in CPL



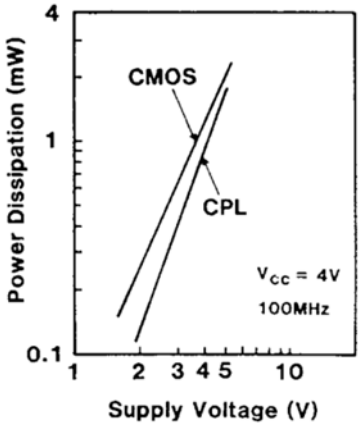
3-input gates designed in CPL

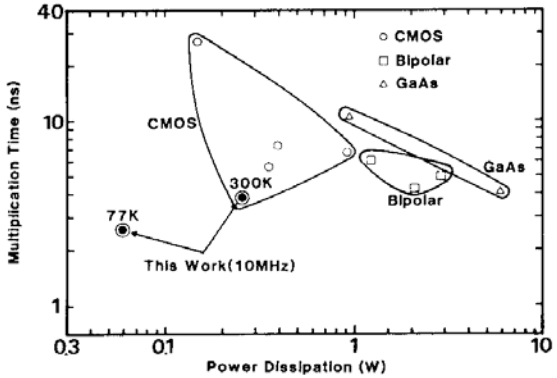


CPL based 1-bit full adder

	CMOS	CPL
Full Adder Circuit		
Transistor Count	40	28
Area	4730μm^2	4218 μm^2
Delay (4V)	0.63ns	0.26ns
Power (100MHz)	1.2mW	0.86mW

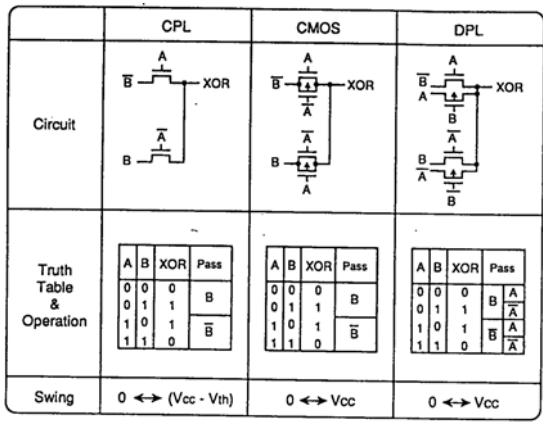
Advantages of CPL



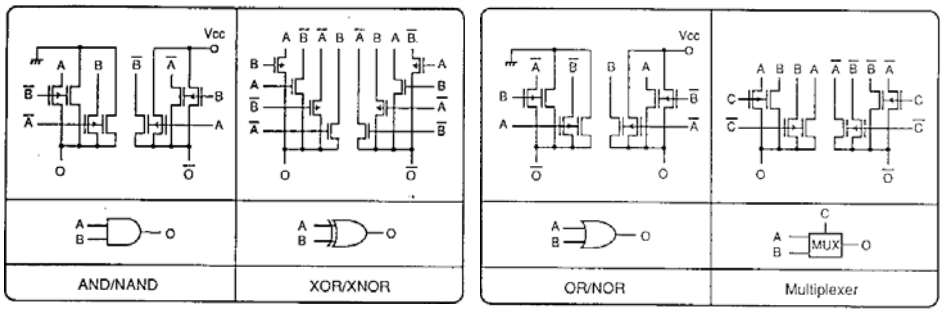


Double Pass-transistor Logic (DPL)

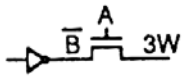
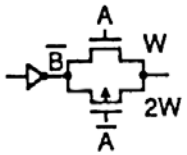
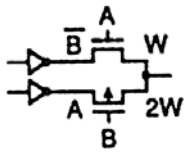
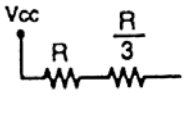
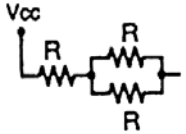
- "A 1.5-ns 32-b CMOS ALU in Double Pass-Transistor Logic", M. Suzuki etc., IEEE J. of Solid-State Circuits, Vol 28, No 11, Nov., 1993



Basic gates in DPL

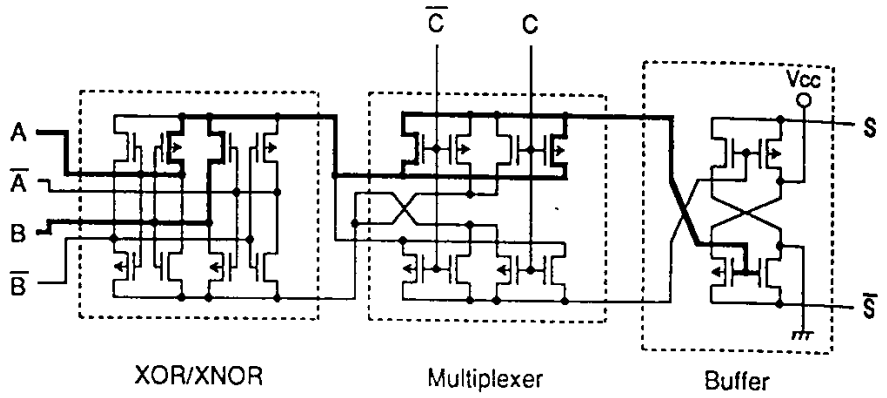


Why is DPL faster?

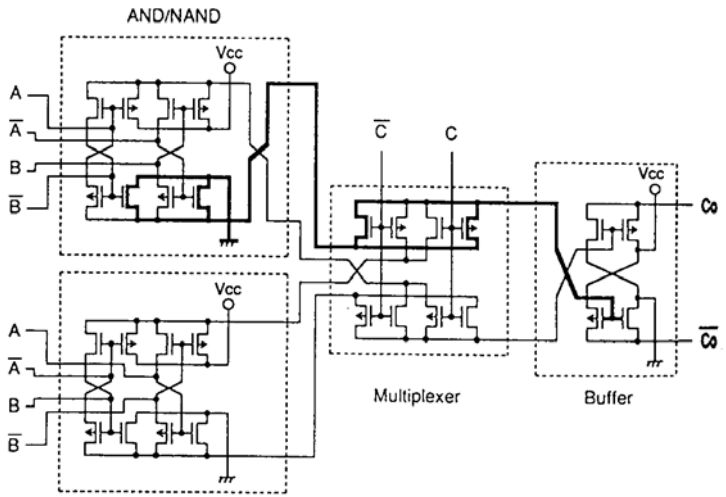
	CPL	CMOS	DPL
Current Path			
Equiv. Circuit			
Equiv. Resistance	$\frac{4}{3}R$	$\frac{3}{2}R$	R

Sum circuit in DPL

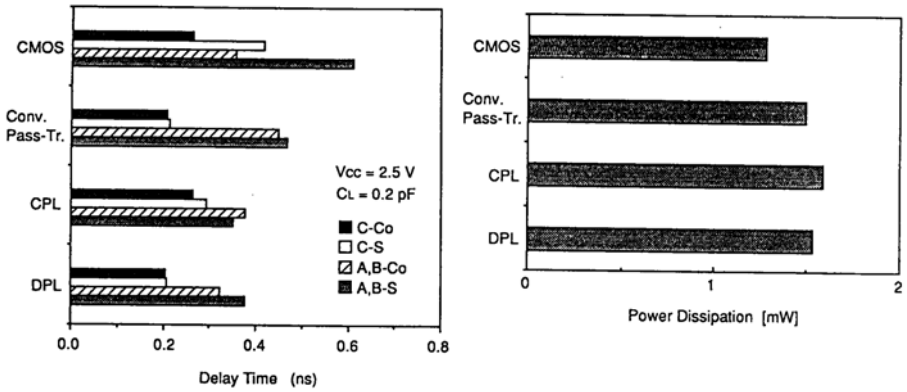
- This adder circuit is extremely elegant. We have shown that for 0.6 micron technology, it offers up to 20% faster operating speed when compare with normal CMOS with only marginal increase in area.



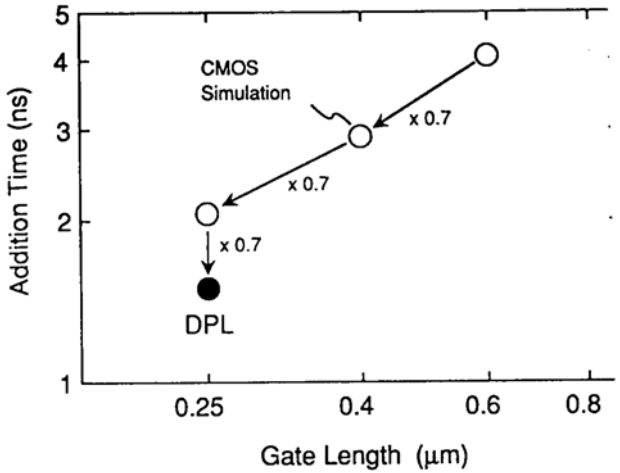
Carry circuit in DPL



Power & Speed of DPL

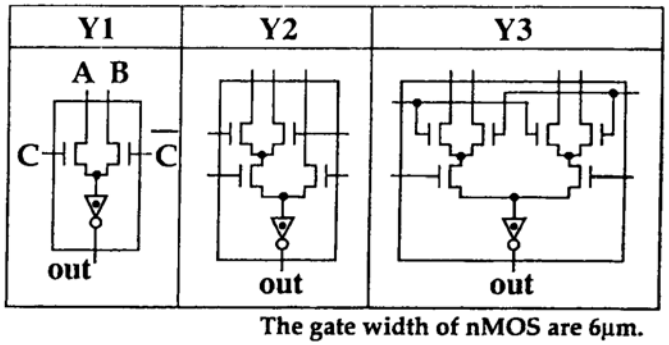


Overall add time of DPL



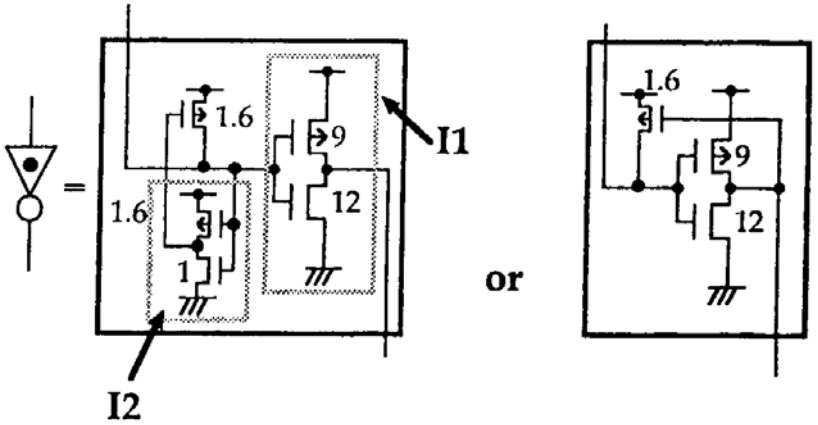
Lean Integration with Pass-Transistor (LEAP)

- "Top-Down Pass-Transistor Logic Design", K. Yano etc., IEEE J. of Solid-State Circuits, Vol 31, No. 6, June 1996.
- It eliminated the need for keeping a large cell library by replacing a library of 61 basic cells with a new set of THREE library cells called Y1, Y2 and Y3, and 4 inverters of different drive strength.



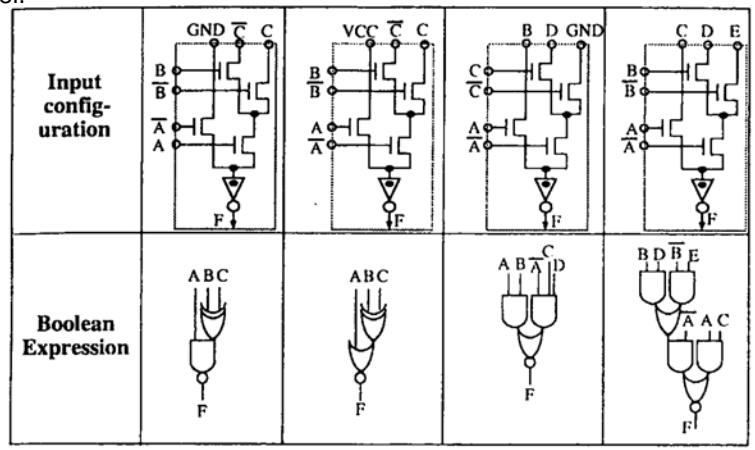
Inverters used in LEAP

- Note that the inverter on the left is used for driving very large output load and the right inverter for normal load capacitance.

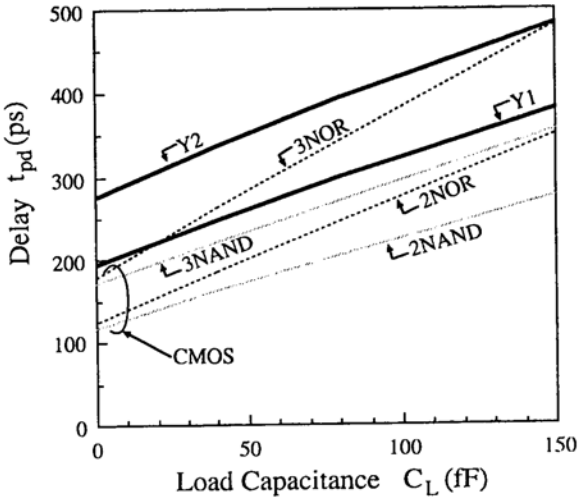


Y2 can be configured for different logic

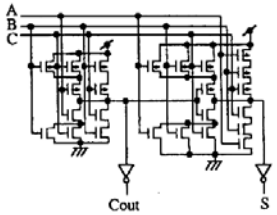
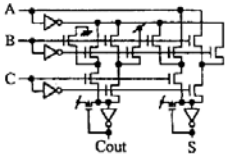
- Arbitrary logic circuits can be implement at almost transistor level, not gate level.



Speed of LEAP



CMOS vs LEAP

Full Adder	Reported Circuits [18, 19]	Circuit Inventor (This Work)
Circuit Diagram		
Tr. Count	28 (1)	24 (0.86)
Area	1810 μm² (1)	1161 μm² (0.64)
Delay	0.73 ns (1)	0.32 ns (0.44)
Power	3.65 μW/MHz (1)	2.35 μW/MHz (0.64)
FOM*	1	6.5